TEXAS INSTRUMENTS

OPA192, OPA2192, OPA4192

SBOS620E – DECEMBER 2013 – REVISED NOVEMBER 2015

OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™

1 Features

- Low Offset Voltage: ±5 µV
- Low Offset Voltage Drift: ±0.2 µV/°C
- Low Noise: 5.5 nV/√Hz at 1 kHz
- High Common-Mode Rejection: 140 dB
- Low Bias Current: ±5 pA
- Rail-to-Rail Input and Output
- Wide Bandwidth: 10 MHz GBW
- High Slew Rate: 20 V/µs
- Low Quiescent Current: 1 mA per Amplifier
- Wide Supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- EMI/RFI Filtered Inputs
- Differential Input Voltage Range to Supply Rail
- High Capacitive Load Drive Capability: 1 nF
- Industry Standard Packages:
  - Single in SOIC-8, SOT-23-5, and VSSOP-8
  - Dual in SOIC-8 and VSSOP-8
  - Quad in SOIC-14 and TSSOP-14

2 Applications

- Multiplexed Data-Acquisition Systems
- Test and Measurement Equipment
- High-Resolution ADC Driver Amplifiers
- SAR ADC Reference Buffers
- Programmable Logic Controllers
- High-Side and Low-Side Current Sensing
- High Precision Comparator

3 Description

The OPAx192 family (OPA192, OPA2192, and OPA4192) is a new generation of 36-V, e-trim operational amplifiers.

These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset (±5 µV, typ), low offset drift (±0.2 µV/°C, typ), and 10-MHz bandwidth.

Unique features such as differential input-voltage range to the supply rail, high output current (±65 mA), high capacitive load drive of up to 1 nF, and high slew rate (20 V/µs) make the OPA192 a robust, high-performance operational amplifier for high-voltage industrial applications.

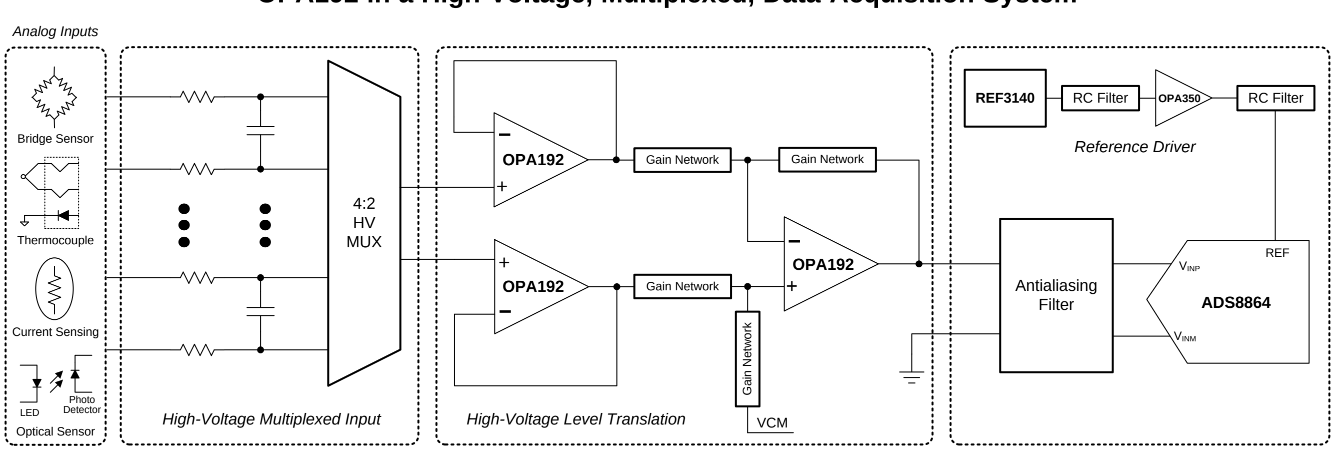
The OPA192 family of op amps is available in standard packages and is specified from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA192	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2192	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4192	SOIC (14)	8.65 mm x 3.90 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPA192 in a High-Voltage, Multiplexed, Data-Acquisition System



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2015) to Revision E — **Page**

- Changed PW package from product preview to production data ... 1
- Added PW package to test condition for input offset voltage drift ... 8
- Added PW package to test condition for input offset voltage drift ... 10
- Added PW package condition to Figure 8 ... 13
- Added PW package condition to Figure 10 ... 13
- Added PW package condition to Figure 52 ... 22
- Changed Figure 70 to fix typos ... 36

Changes from Revision C (March 2015) to Revision D — **Page**

- Changed device status to Production Data; OPA4192 released to Production ... 1
- Deleted footnote 2 from *Device Information* table ... 1
- Deleted footnote 2 from *Pin Configuration and Functions* section ... 4
- Changed *ESD Ratings* table: added correct OPA4192 CDM specifications ... 6
- Added Frequency Response, *Crosstalk* parameter to *Electrical Characteristics: V_S = ±4 V to ±18 V* table ... 9
- Added Frequency Response, *Crosstalk* parameter to *Electrical Characteristics: V_S = ±2.25 V to ±4 V* table ... 11
- Changed *Typical Characteristics* to current standards (split curves and table of graphs into separate sections to be SDS compliant) ... 12
- Added *Crosstalk vs Frequency* row to Table 1 ... 12
- Added Figure 48 ... 20

Changes from Revision B (March 2014) to Revision C — **Page**

- Added CDM row for OPA2192, OPA4192 in ESD Ratings table 6
- Changed input offset voltage values for $V_{CM} \geq (V+) - 1.5$ V test condition 8
- Changed Input offset voltage parameter typical specs for $V_{CM} = (V+) - 1.5$ V test conditions 8
- Changed test conditions for dV_{OS}/dT parameter 8
- Changed input offset voltage max values and test conditions for $V_{CM} = (V+) - 3$ V test condition 10
- Changed input offset voltage values and test conditions for $V_{CM} = (V+) - 1.5$ V test condition 10
- Changed Input offset voltage parameter typical specs for $V_{CM} = (V+) - 1.5$ V test conditions 10
- Changed test conditions for dV_{OS}/dT parameter 10
- Added text to last bullet of *Layout Guidelines* section 35

Changes from Revision A (January 2014) to Revision B — **Page**

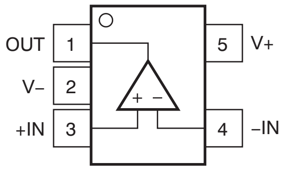
- Added ESD Ratings and Recommended Operating Conditions tables, and *Parameter Measurement Information*, *Application and Implementation*, *Power-Supply Recommendations*, and *Device and Documentation Support* sections, and moved existing sections 1
- Changed all OPA192 and OPA2192 packages to production data 1
- Changed package names to latest standard; changed all MSOP to VSSOP, SO to SOIC, and SOT23 to SOT 1
- Deleted DCK package pin configuration 4
- Added thermal information for OPA192 DBV and DGK packages 7
- Added OPA2192 and OPA4192 Thermal Information tables 7
- Added rows with additional test conditions to input offset voltage parameter 8
- Changed Input offset voltage drift parameter 8
- Changed CMRR test conditions 8
- Added rows with additional test conditions to input offset voltage parameter 10
- Changed Input offset voltage drift parameter 10
- Changed PSSR parameter 10
- Changed CMRR test conditions 10
- Added *Output* section 11
- Added typical characteristic curves to Table 1 12
- Added $T_A = 25°C$ to Typical Characteristics condition line 12
- Added nine new histogram plots from Figure 2 to Figure 10 13
- Changed Figure 11 to show more units 13
- Changed Figure 19 15
- Added text to *Application Information* section 31
- Changed text in *Layout Guidelines* section 35

Changes from Original (December 2013) to Revision A — **Page**

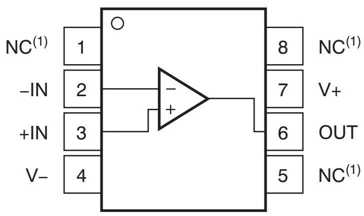
- Changed first paragraph of *16-Bit Precision Multiplexed Data-Acquisition System* section 31
- Changed Figure 66 and title 31
- Changed TIDU181 reference design title 32

5 Pin Configuration and Functions

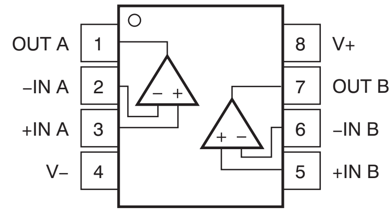
DBV Package: OPA192
5-Pin SOT
Top View



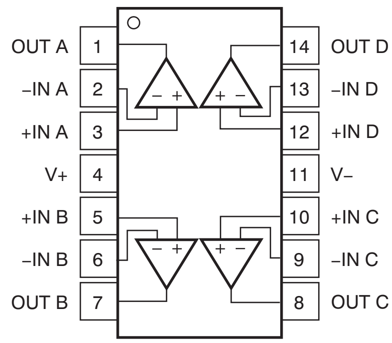
D and DGK Packages: OPA192
8-Pin SOIC and VSSOP
Top View



D and DGK Packages: OPA2192
8-Pin SOIC and VSSOP
Top View



D and PW Packages: OPA4192
14-Pin SOIC and TSSOP
Top View



(1) NC = No internal connection.

Pin Functions: OPA192

PIN			I/O	DESCRIPTION
NAME	OPA192			
	D (SOIC), DGK (VSSOP)	DBV (SOT)		
+IN	3	3	I	Noninverting input
–IN	2	4	I	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

Pin Functions: OPA2192 and OPA4192

PIN			I/O	DESCRIPTION
NAME	OPA2192	OPA4192		
	D (SOIC), DGK (VSSOP)	D (SOIC), PW (TSSOP)		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input,,channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	—	Positive (highest) power supply
V–	4	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				±20 (40, single supply)	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit[2]			Continuous		
Temperature	Operating range		–55	150	°C
	Junction			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
OPA192				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	V
OPA2192				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	V
OPA4192				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		+125	°C

6.4 Thermal Information: OPA192

THERMAL METRIC(1)		OPA192			UNIT
		D (SOIC)	DBV (SOT)	DGK (VSSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	158.8	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	60.1	60.7	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	44.8	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	1.6	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	4.2	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2192

THERMAL METRIC(1)		OPA2192		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.9	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.3	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information: OPA4192

THERMAL METRIC(1)		OPA4192		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.3	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = +8 V to +36 V)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = 0°C to 85°C			±8	±50	µV
		T_A = –40°C to +125°C			±10	±75	µV
		V_{CM} = (V+) – 1.5 V			±10	±40	µV
		V_{CM} = (V+) – 1.5 V	T_A = 0°C to 85°C		±25	±150	µV
		V_{CM} = (V+) – 1.5 V	T_A = –40°C to +125°C		±50	±250	µV
dV_{OS}/dT	Input offset voltage drift	D packages only	T_A = 0°C to 85°C		±0.1	±0.5	µV/°C
		D packages only	T_A = –40°C to +125°C		±0.15	±0.8	µV/°C
		DBV, DGK, and PW packages only	T_A = 0°C to 85°C		±0.1	±0.8	µV/°C
		DBV, DGK, and PW packages only	T_A = –40°C to +125°C		±0.2	±1.0	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.30		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		μV_{PP}
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		nV/√Hz
		(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 1 kHz		5.5		nV/√Hz
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		nV/√Hz
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 1 kHz		12.5		nV/√Hz
NOISE (continued)							
i_n	Input current noise density	f = 1 kHz			1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
		(V–) – 0.1 V < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	114	126		dB
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		dB
		(V+) – 1.5 V < V_{CM} < (V+)	T_A = –40°C to +125°C	86	100		dB
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		120	134		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ	T_A = –40°C to +125°C	114	126		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		126	140		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ	T_A = –40°C to +125°C	120	134		dB

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = +8 V to +36 V) (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.4		µs
			V_S = ±18 V, G = 1, 5-V step		0.9		
		To 0.001%	V_S = ±18 V, G = 1, 10-V step		2.1		
			V_S = ±18 V, G = 1, 5-V step		1.8		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008%		
	Crosstalk	OPA2192 and OPA4192, at dc			150		dB
		OPA2192 and OPA4192, f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 31			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
		T_A = –40°C to +125°C, I_O = 0 A				1.5	
TEMPERATURE							
	Thermal protection (1)				140		°C

(1) For a detailed description of thermal protection, see the *Thermal Protection* section.

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = +4.5 V to +8 V)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3 V			±5	±25	µV
			T_A = 0°C to 85°C		±8	±50	µV
			T_A = –40°C to +125°C		±10	±75	µV
		(V+) – 3.5 V < V_{CM} < (V+) – 1.5 V		See *Common-Mode Voltage Range* section			
		V_{CM} = (V+) – 1.5 V			±10	±40	µV
			T_A = 0°C to 85°C		±25	±150	µV
			T_A = –40°C to +125°C		±50	±250	µV
dV_{OS}/dT	Input offset voltage drift	V_{CM} = (V+) – 3 V, D packages only	T_A = 0°C to 85°C		±0.1	±0.5	µV/°C
			T_A = –40°C to +125°C		±0.15	±0.8	µV/°C
		V_{CM} = (V+) – 3 V, DBV, DGK, and PW packages only	T_A = 0°C to 85°C		±0.1	±0.8	µV/°C
			T_A = –40°C to +125°C		±0.2	±1.1	µV/°C
		V_{CM} = (V+) – 1.5 V, T_A = –40°C to +125°C			±0.5	±3	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C, V_{CM} = V_S / 2 – 0.75 V			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V, f = 0.1 Hz to 10 Hz			1.30		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V, f = 0.1 Hz to 10 Hz			4		$µV_{PP}$
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		nV/√Hz
			f = 1 kHz		5.5		nV/√Hz
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		nV/√Hz
			f = 1 kHz		12.5		nV/√Hz
i_n	Input current noise density		f = 1 kHz		1.5		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		94	110		dB
			T_A = –40°C to +125°C	90	104		dB
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		dB
			T_A = –40°C to +125°C	84	100		dB
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		110	120		dB
			T_A = –40°C to +125°C	100	114		dB
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		110	126		dB
			T_A = –40°C to +125°C	110	120		dB

Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = +4.5 V to +8 V) (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±3 V, G = 1, 5-V step		1		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
	Crosstalk	OPA2192 and OPA4192, at dc			150		dB
		OPA2192 and OPA4192, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 31			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
			T_A = –40°C to +125°C			1.5	
TEMPERATURE							
	Thermal protection (1)				140		°C

(1) For a detailed description of thermal protection, see the *Thermal Protection* section.

6.9 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1 to Figure 6
Offset Voltage Drift Distribution	Figure 7 to Figure 10
Offset Voltage vs Temperature	Figure 11
Offset Voltage vs Common-Mode Voltage	Figure 12 to Figure 14
Offset Voltage vs Power Supply	Figure 15
Open-Loop Gain and Phase vs Frequency	Figure 16
Closed-Loop Gain and Phase vs Frequency	Figure 17
Input Bias Current vs Common-Mode Voltage	Figure 18
Input Bias Current vs Temperature	Figure 19
Output Voltage Swing vs Output Current (maximum supply)	Figure 20
CMRR and PSRR vs Frequency	Figure 21
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PSRR vs Temperature	Figure 23
0.1-Hz to 10-Hz Noise	Figure 24
Input Voltage Noise Spectral Density vs Frequency	Figure 25
THD+N Ratio vs Frequency	Figure 26
THD+N vs Output Amplitude	Figure 27
Quiescent Current vs Supply Voltage	Figure 28
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Open Loop Gain vs Temperature	Figure 30
Open Loop Output Impedance vs Frequency	Figure 31
Small Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 32, Figure 33
No Phase Reversal	Figure 34
Positive Overload Recovery	Figure 35
Negative Overload Recovery	Figure 36
Small-Signal Step Response (100 mV)	Figure 37, Figure 38
Large-Signal Step Response	Figure 39
Settling Time	Figure 40 to Figure 43
Short-Circuit Current vs Temperature	Figure 44
Maximum Output Voltage vs Frequency	Figure 45
Propagation Delay Rising Edge	Figure 46
Propagation Delay Falling Edge	Figure 47
Crosstalk vs Frequency	Figure 48

6.10 Typical Characteristics

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

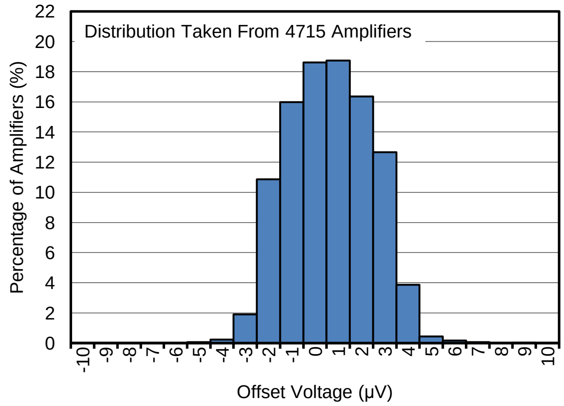


Figure 1. Offset Voltage Production Distribution at 25°C

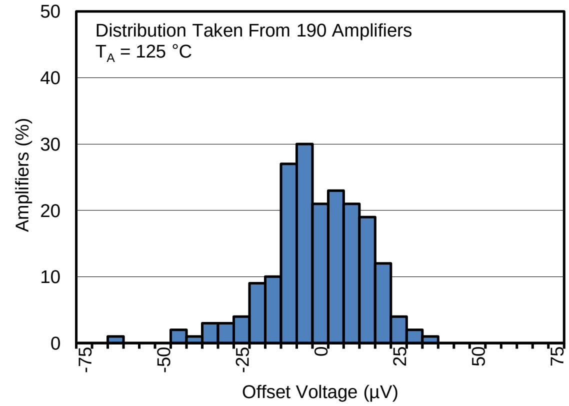


Figure 2. Offset Voltage Production Distribution at 125°C

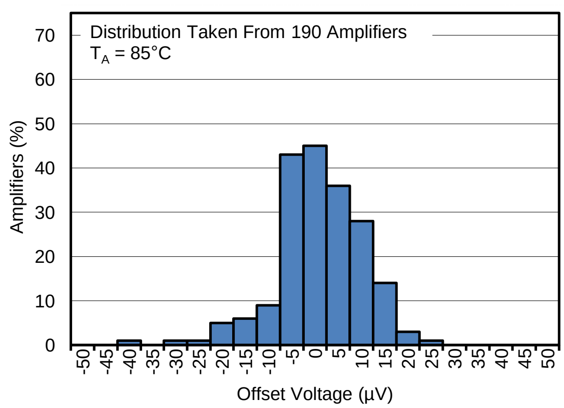


Figure 3. Offset Voltage Production Distribution at 85°C

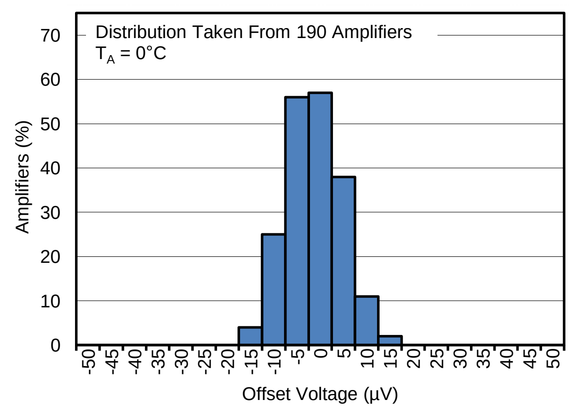


Figure 4. Offset Voltage Production Distribution at 0°C

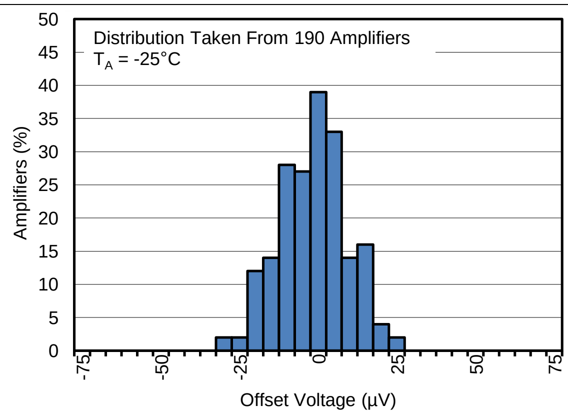


Figure 5. Offset Voltage Production Distribution at –25°C

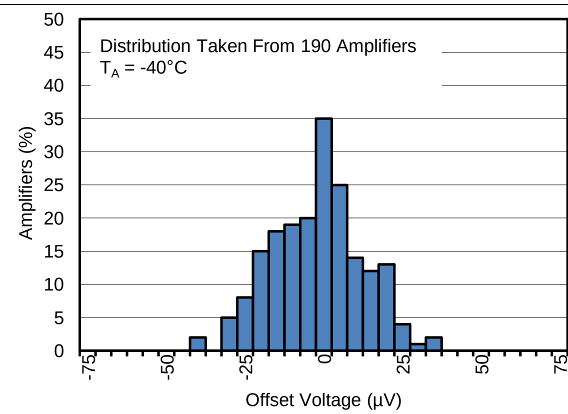
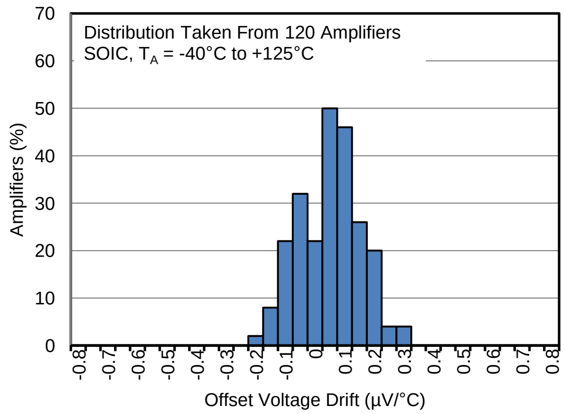


Figure 6. Offset Voltage Production Distribution at –40°C

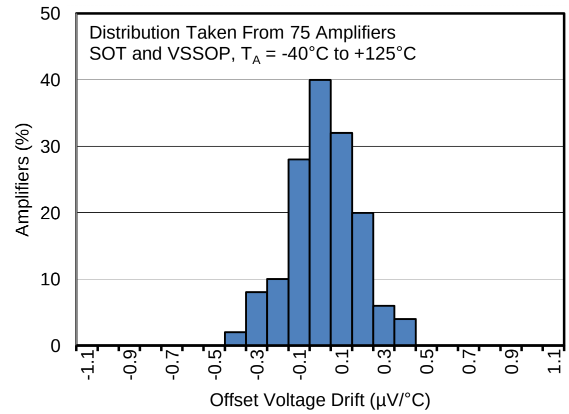
Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



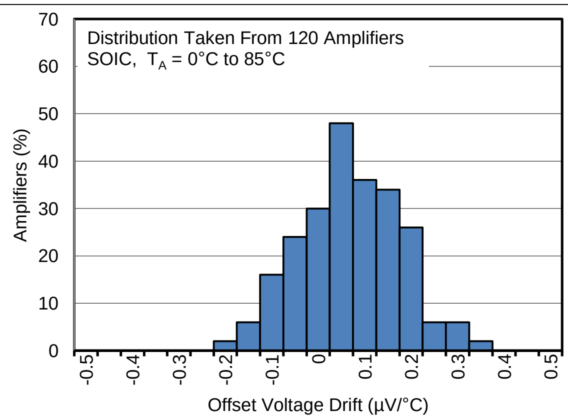
OPA192ID and OPA2192ID

Figure 7. Offset Voltage Drift Distribution from –40°C to +125°C



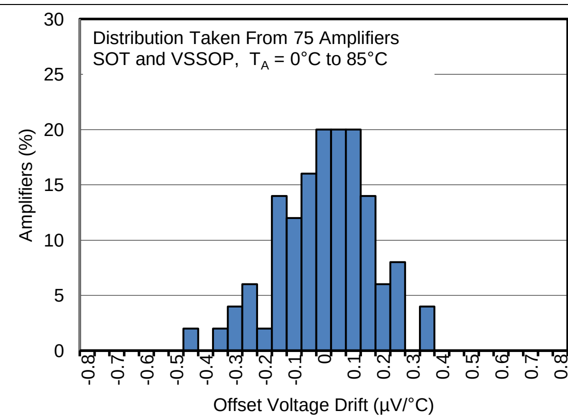
OPA192IDBV, OPA192IDGK, OPA2192IDGK, and OPA4192IPW

Figure 8. Offset Voltage Drift Distribution from –40°C to +125°C



OPA192ID and OPA2192ID

Figure 9. Offset Voltage Drift Distribution from 0°C to 85°C



OPA192IDBV, OPA192IDGK, OPA2192IDGK, and OPA4192IPW

Figure 10. Offset Voltage Drift Distribution from 0°C to 85°C

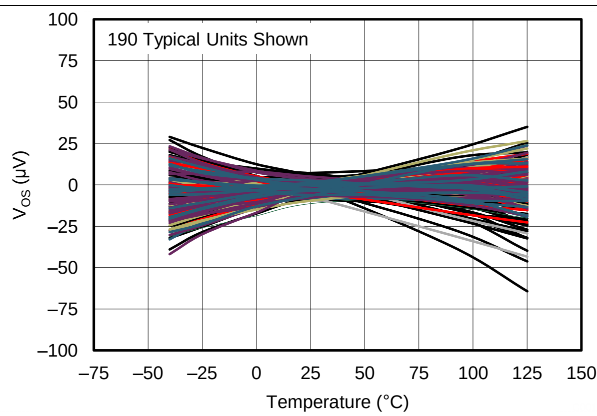


Figure 11. Offset Voltage vs Temperature

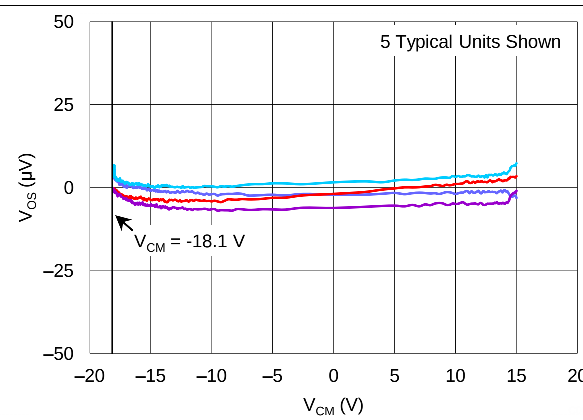


Figure 12. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

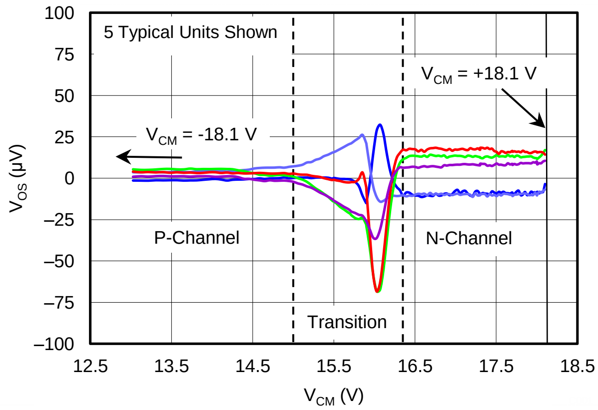


Figure 13. Offset Voltage vs Common-Mode Voltage

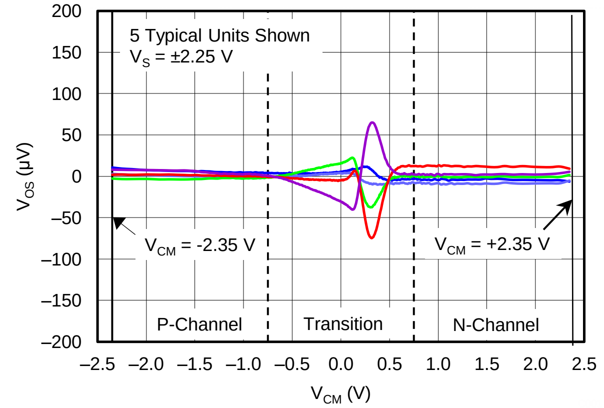


Figure 14. Offset Voltage vs Common-Mode Voltage

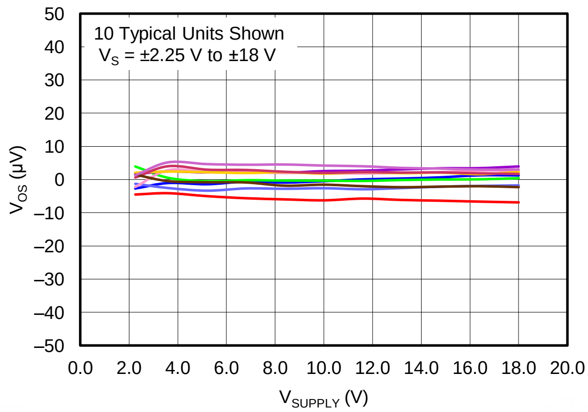


Figure 15. Offset Voltage vs Power Supply

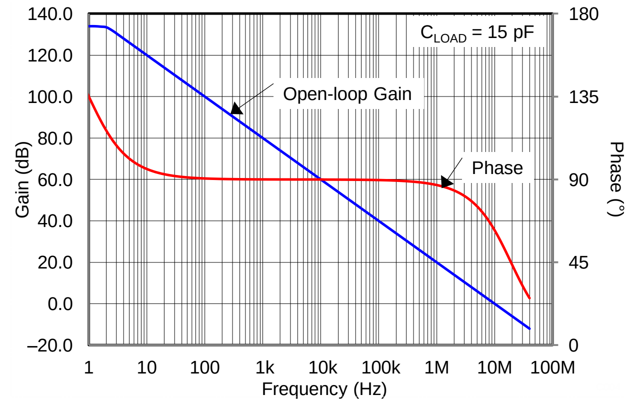


Figure 16. Open-Loop Gain and Phase vs Frequency

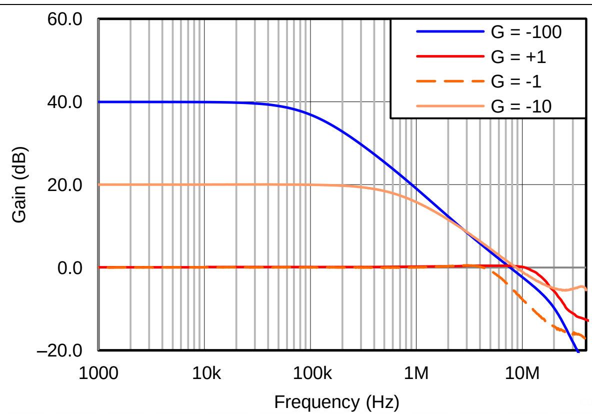


Figure 17. Closed-Loop Gain and Phase vs Frequency

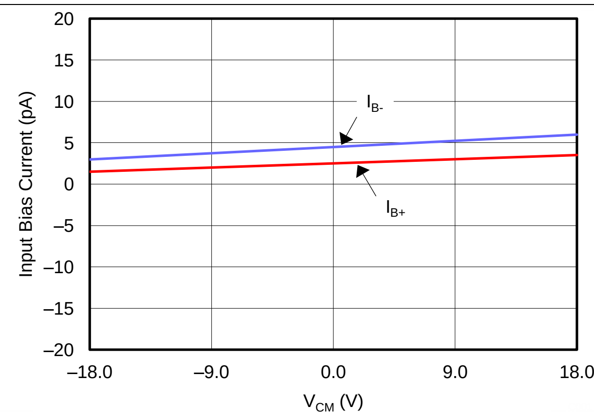


Figure 18. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

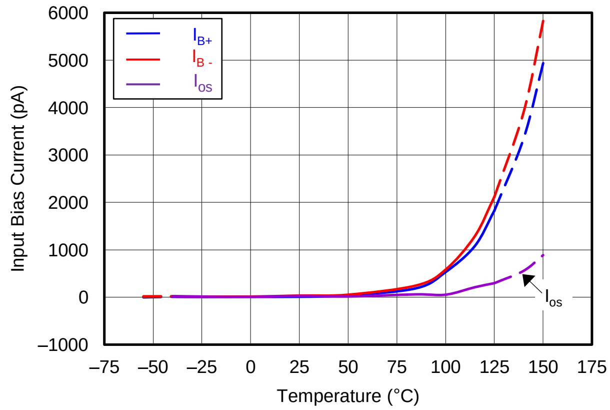


Figure 19. Input Bias Current vs Temperature

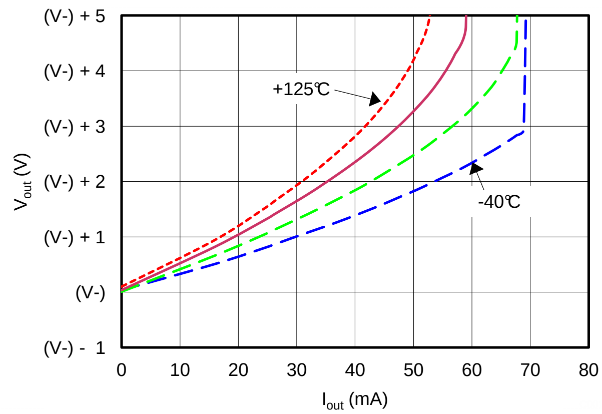


Figure 20. Output Voltage Swing vs Output Current (Maximum Supply)

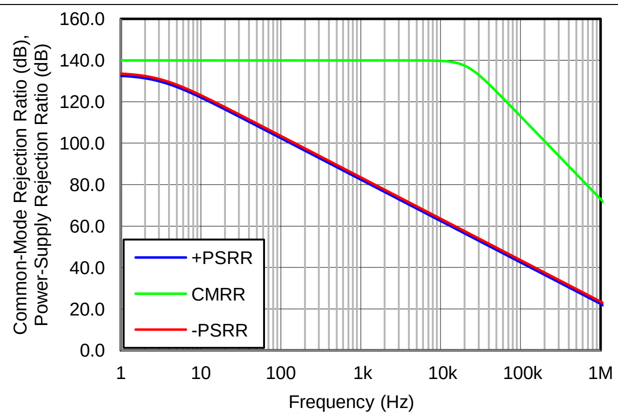


Figure 21. CMRR and PSRR vs Frequency

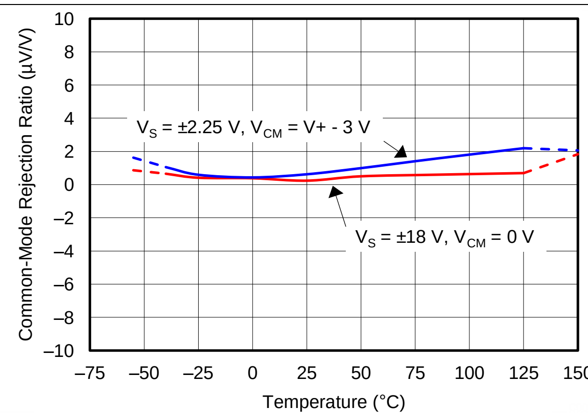


Figure 22. CMRR vs Temperature

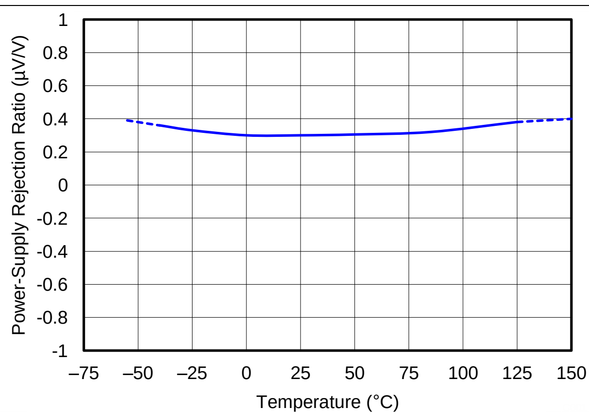


Figure 23. PSRR vs Temperature

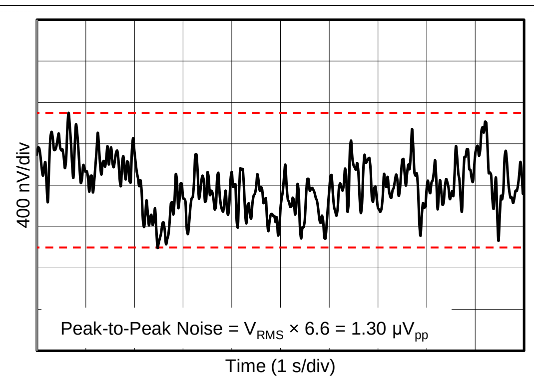


Figure 24. 0.1-Hz to 10-Hz Noise

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

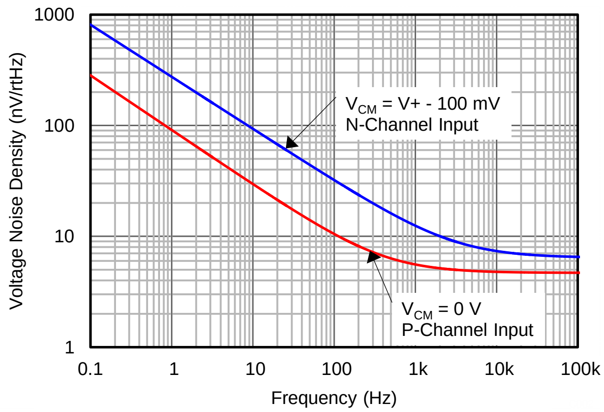


Figure 25. Input Voltage Noise Spectral Density vs Frequency

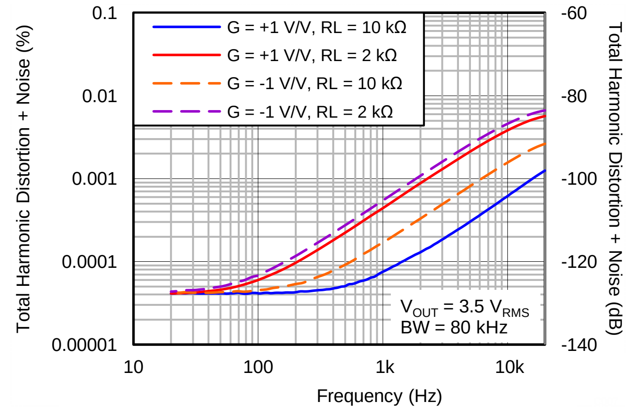


Figure 26. THD+N Ratio vs Frequency

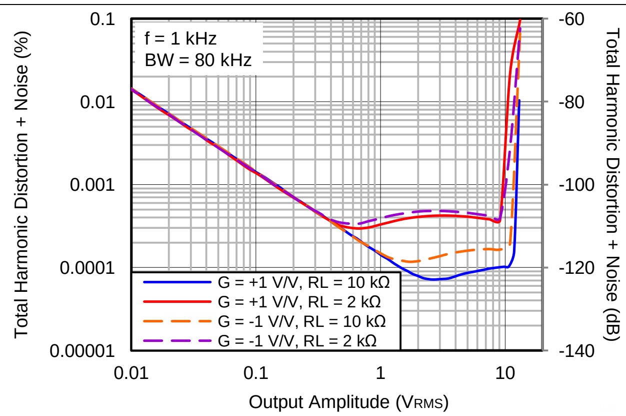


Figure 27. THD+N vs Output Amplitude

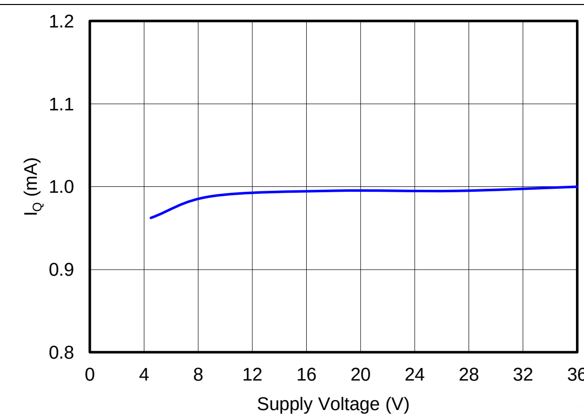


Figure 28. Quiescent Current vs Supply Voltage

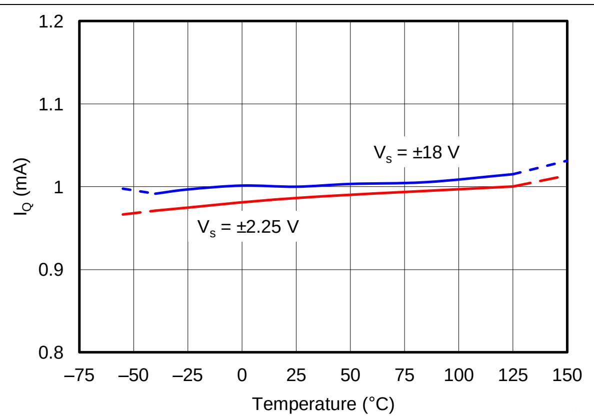


Figure 29. Quiescent Current vs Temperature

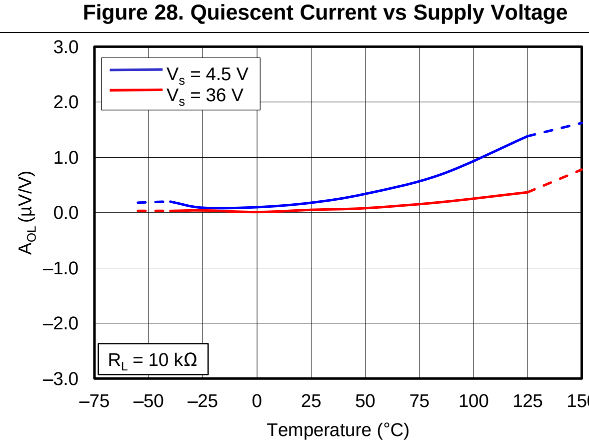


Figure 30. Open-Loop Gain vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

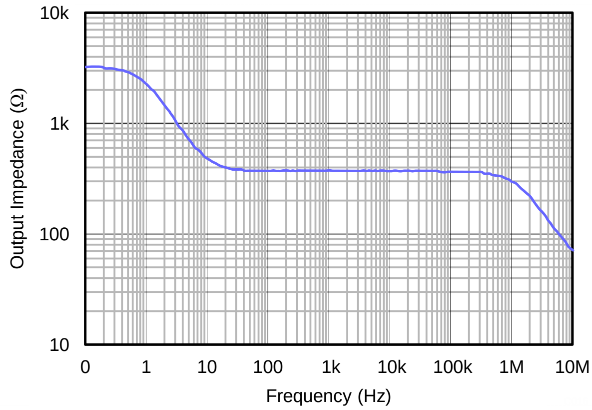


Figure 31. Open-Loop Output Impedance vs Frequency

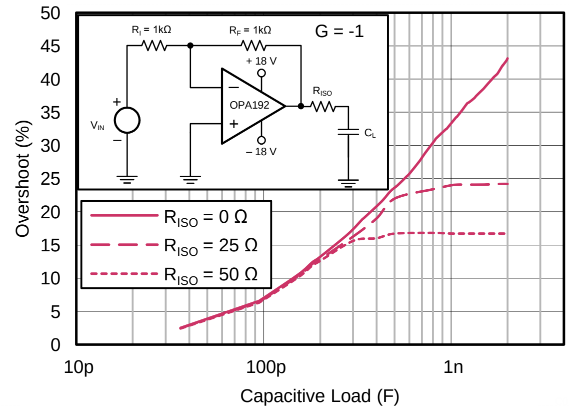


Figure 32. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

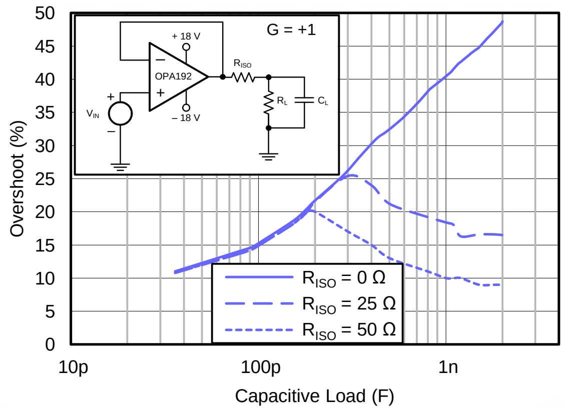


Figure 33. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

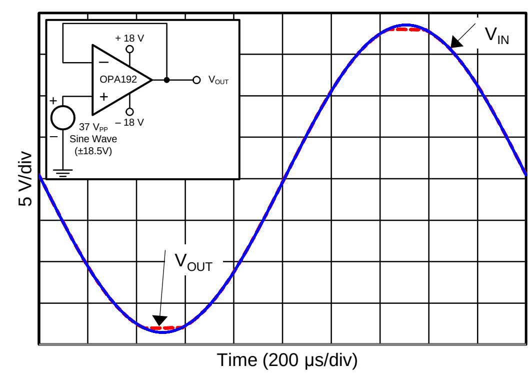


Figure 34. No Phase Reversal

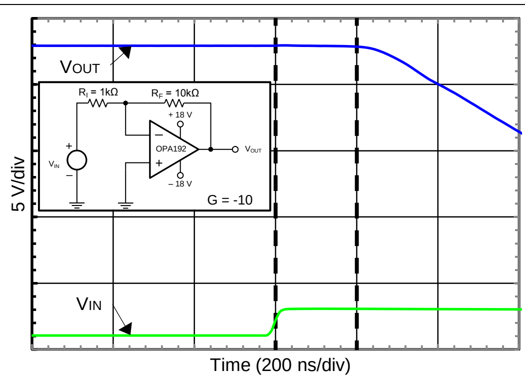


Figure 35. Positive Overload Recovery

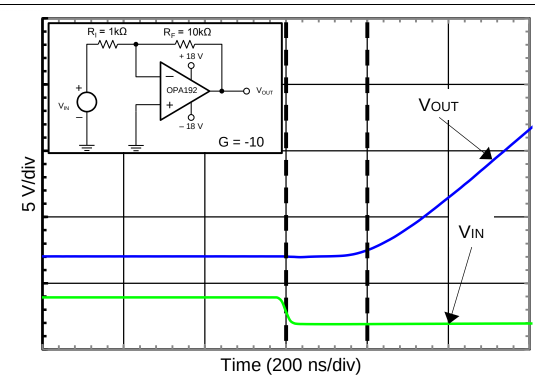


Figure 36. Negative Overload Recovery

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

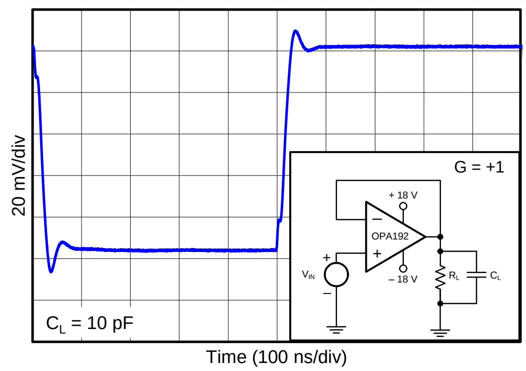


Figure 37. Small-Signal Step Response (100 mV)

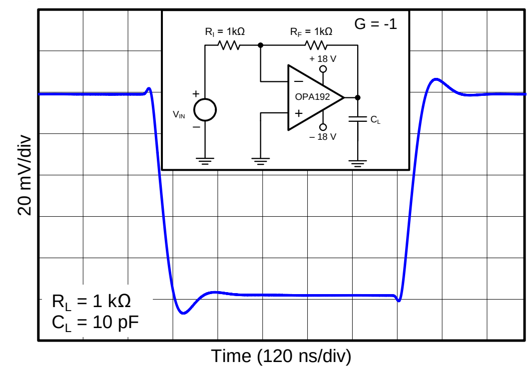


Figure 38. Small-Signal Step Response (100 mV)

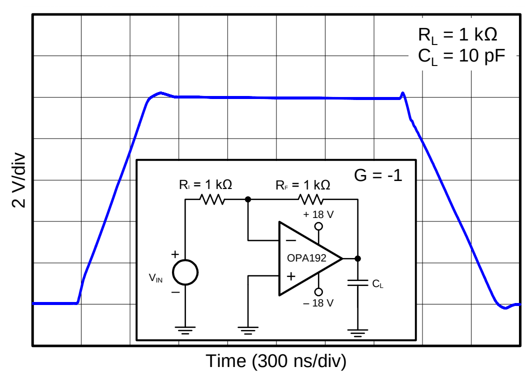


Figure 39. Large-Signal Step Response

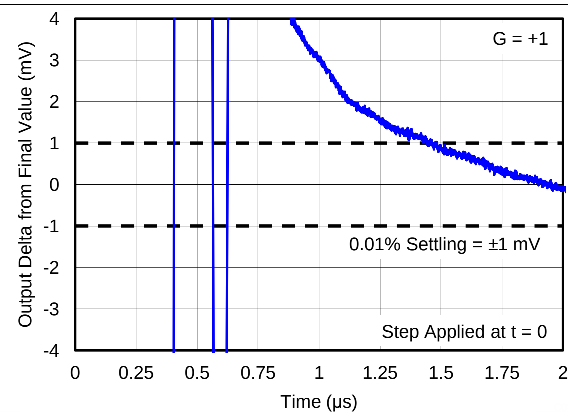


Figure 40. Settling Time (10-V Positive Step)

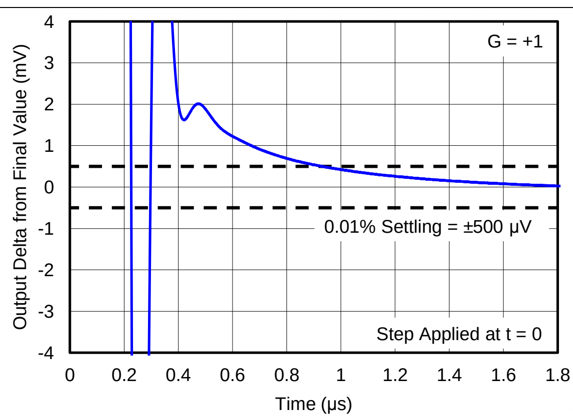


Figure 41. Settling Time (5-V Positive Step)

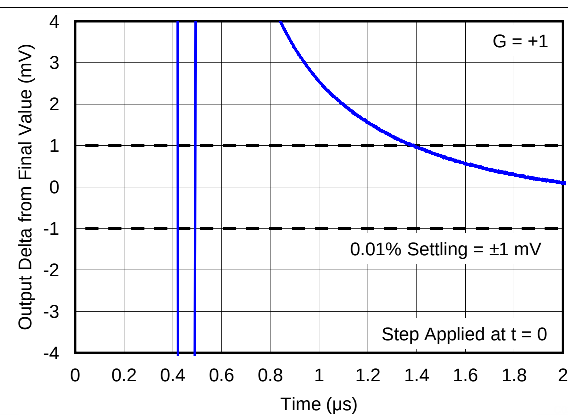


Figure 42. Settling Time (10-V Negative Step)

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

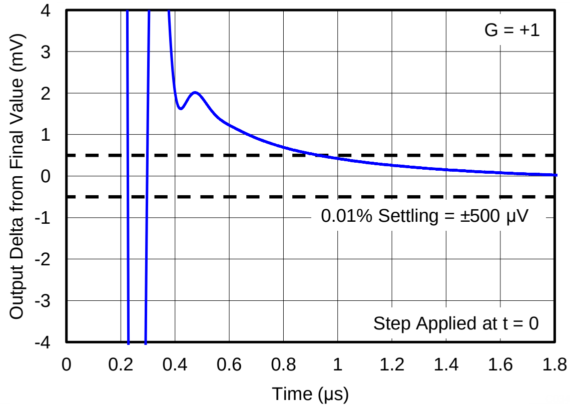


Figure 43. Settling Time (5-V Negative Step)

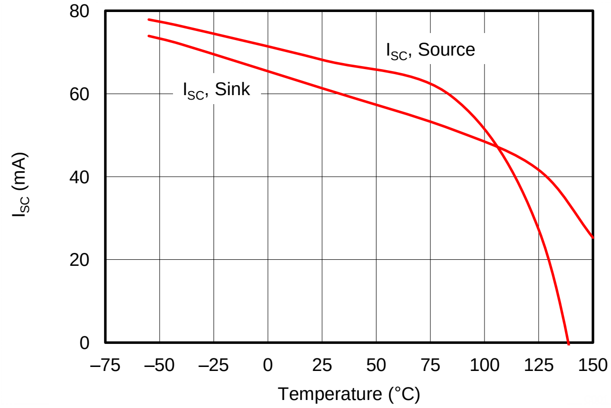


Figure 44. Short-Circuit Current vs Temperature

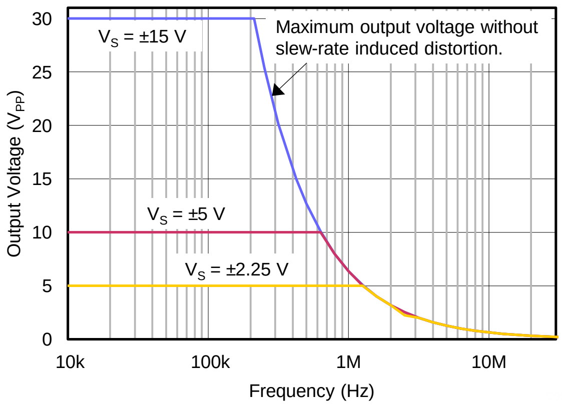


Figure 45. Maximum Output Voltage vs Frequency

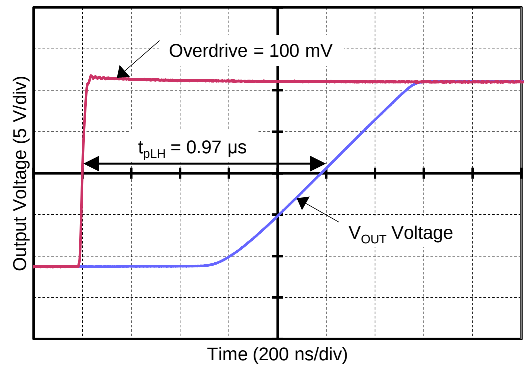


Figure 46. Propagation Delay Rising Edge

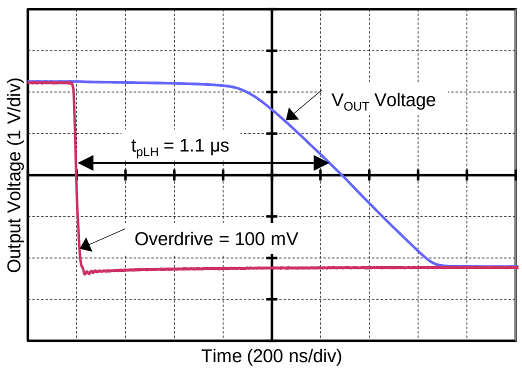


Figure 47. Propagation Delay Falling Edge

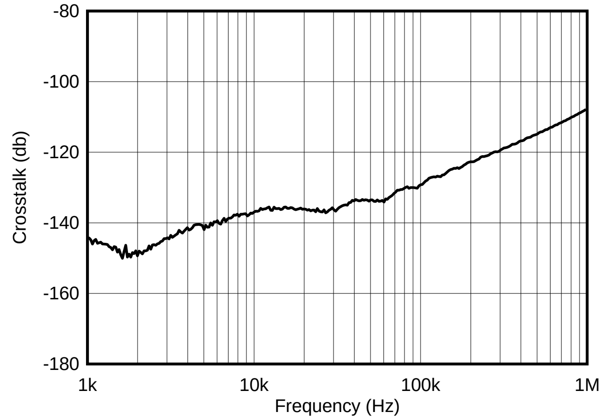


Figure 48. Crosstalk vs Frequency

7 Parameter Measurement Information

7.1 Input Offset Voltage Drift

The OPAx192 family of operational amplifiers is manufactured using TI's e-trim technology. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. When trimming input offset voltage drift the systematic or linear drift error on each device is trimmed to zero. This results in the remaining errors associated with input offset drift are minimal and are the result from only nonlinear error sources. Figure 49 illustrates this concept.

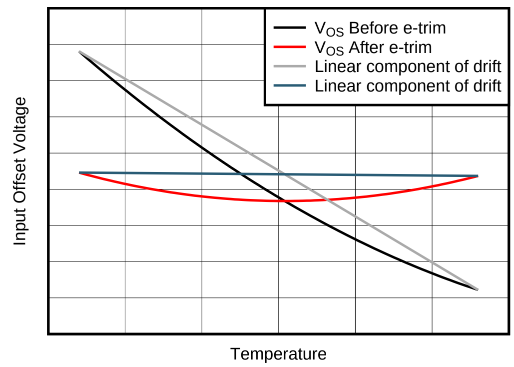


Figure 49. Input Offset Before and After Drift Trim

A common method of specifying input offset voltage drift is the *box method*. The box method estimates a maximum input offset drift by bounding the offset voltage versus temperature curve with a box and using the corners of this bounding box to determine the drift. The slope of the line connecting the diagonal corners of the box corresponds to the input offset voltage drift. Figure 50 shows the box method concept. The box method works particularly well when the input offset drift is dominated by the linear component of drift, but because the OPA192 family uses TI's e-trim technology to remove the linear component input offset voltage drift, the box method is not a particularly useful method of accurately performing an error analysis. Figure 50 shows 30 typical units of the OPAx192 with the box method superimposed for illustrative purposes. The boundaries of the box are determined by the specified temperature range along the x-axis and the maximum specified input offset voltage across that same temperature range along the y-axis. Using the box method predicts an input offset voltage drift of 0.9 µV/°C. As shown in Figure 50, the slopes of the actual input offset voltage versus temperature are much less than that predicted by the box method. The box method predicts a pessimistic value for the maximum input offset voltage drift and is not recommended when performing an error analysis.

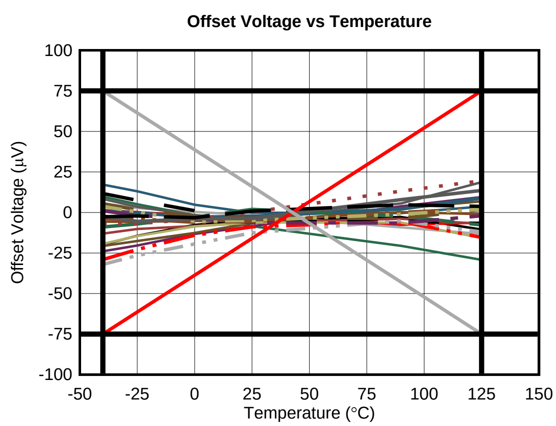


Figure 50. The Box Method

Input Offset Voltage Drift (continued)

Instead of the box method, a convenient way to illustrate input offset drift is to compute the slopes of the input offset voltage versus temperature curve. This is the same as computing the input offset drift at each point along the input offset voltage versus temperature curve. The results for the OPAx192 family are shown in Figure 51 and Figure 52.

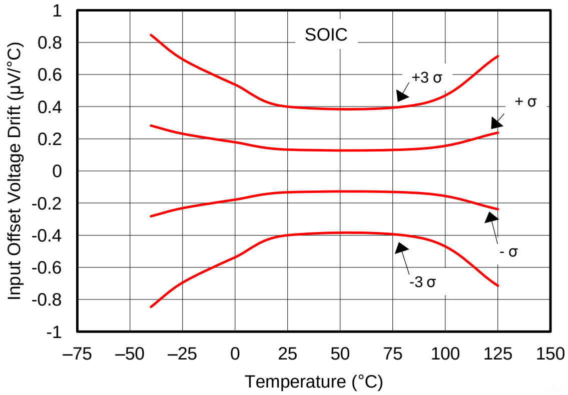


Figure 51. Input Offset Voltage Drift vs Temperature (OPA192ID and OPA2192ID)

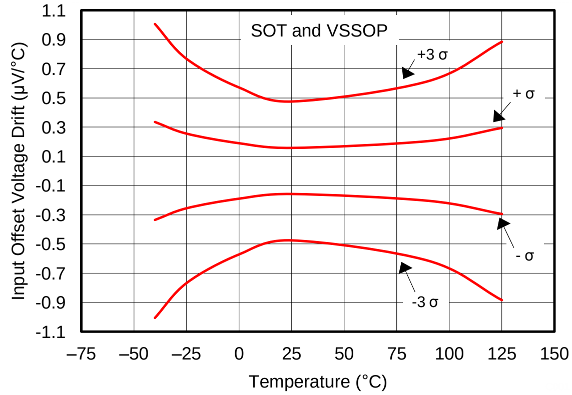


Figure 52. Input Offset Voltage Drift vs Temperature (OPA192IDBV, OPA192IDGK, OPA2192IDGK, and OPA4192IPW)

As shown in Figure 51, the input offset drift is typically less than ±0.3 µV/°C over the range from –40°C to +125°C. When performing an error analysis over the full specified temperature range, use the typical and maximum values for input offset voltage drift as described in the *Electrical Characteristics* tables. If a reduced temperature range is applicable, use the information shown in Figure 51 or Figure 52 when performing an error analysis. To determine the change in input offset voltage, use Equation 1:

$$\Delta V_{OS} = \Delta T \times dV_{OS}/dT \quad (1)$$

where

- ΔV_{OS} = Change in input offset voltage
- ΔT = Change in temperature
- dV_{OS}/dT = Input offset voltage drift

For example, determine the amount of OPA192ID input offset voltage change over the temperature range of 25°C to 75°C for 1 σ (68%) of the units. As shown in Figure 51, the input offset drift is typically 0.15 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.15 µV/°C = 7.5 µV .

For 3 σ (99.7%) of the units, Figure 51 shows a typical input offset drift of 0.4 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.4 µV/°C = 20 µV.

Figure 53 shows six typical units.

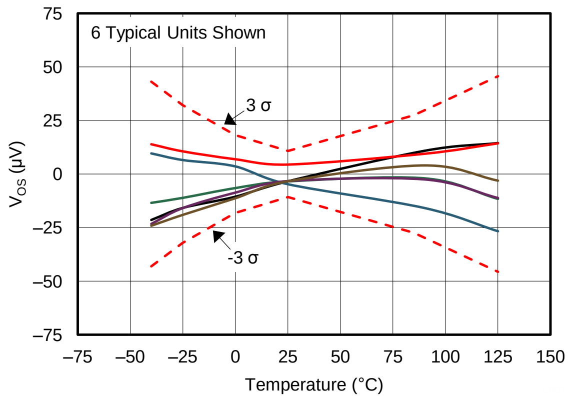


Figure 53. Input Offset Voltage Drift vs Temperature for Six Typical Units

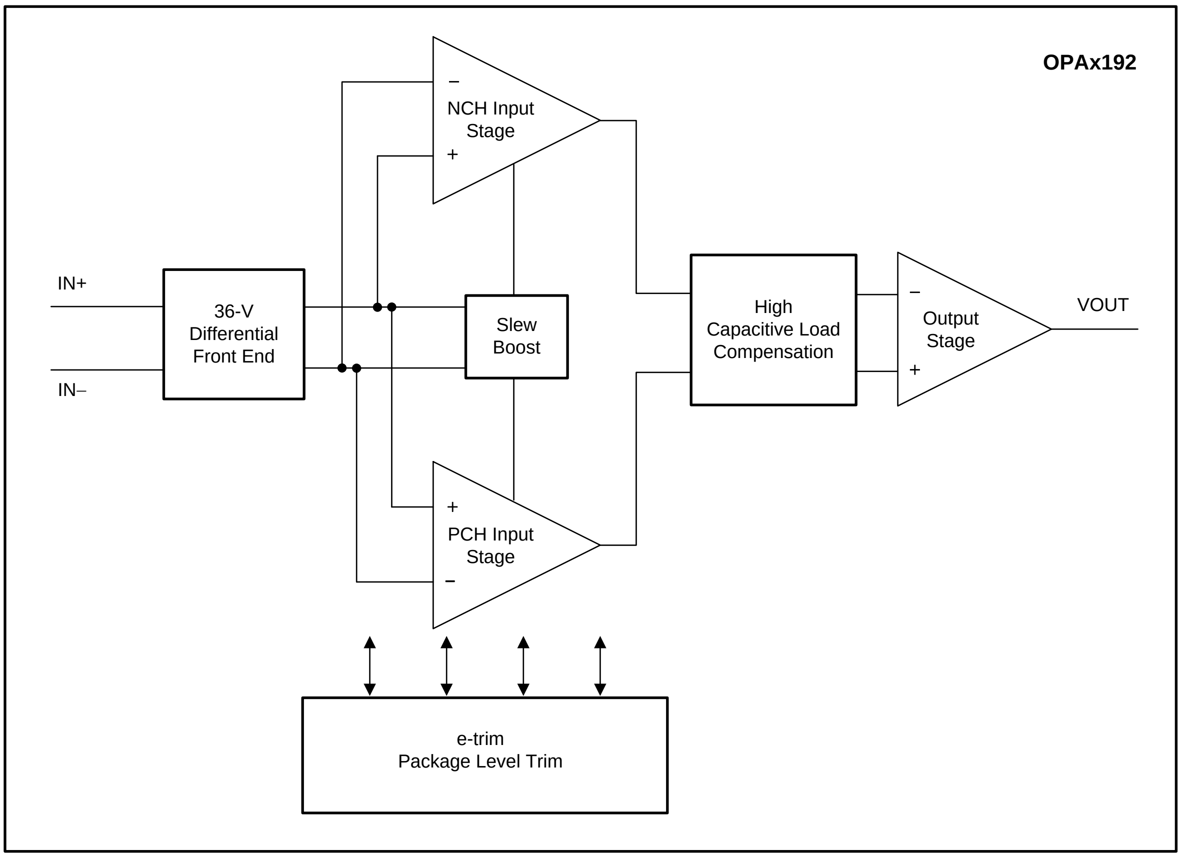
8 Detailed Description

8.1 Overview

The OPAx192 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The *Functional Block Diagram* section shows the simplified diagram of the OPA192 with e-trim.

Unlike previous e-trim op amps, the OPAx192 uses a patented two-temperature trim architecture to achieve a very low offset voltage of 25 µV (max) and low voltage offset drift of 0.5 µV/°C (max) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Protection Circuitry

The OPAx192 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 54 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 55. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current, and resulting in extended settling time, as shown in Figure 56.

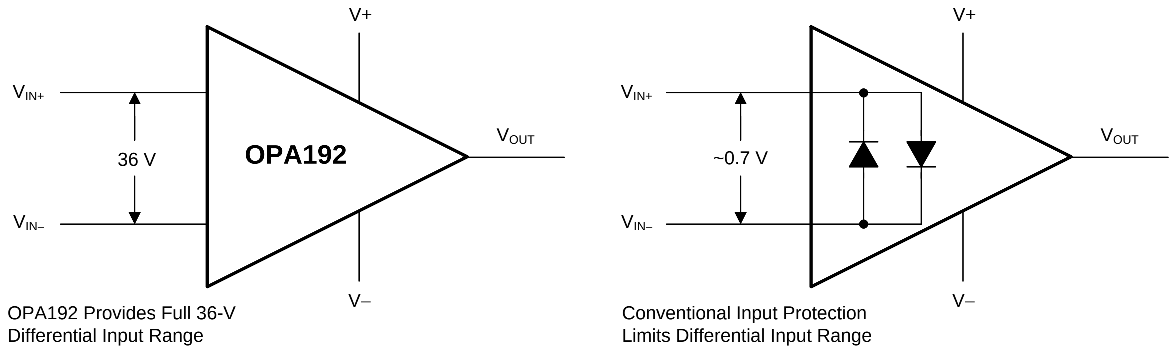


Figure 54. OPA192 Input Protection Does Not Limit Differential Input Capability

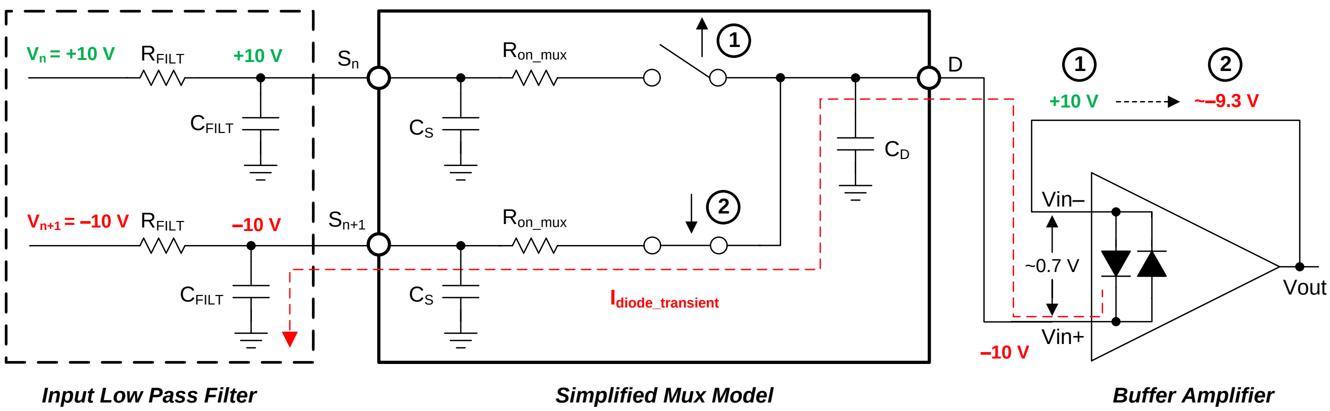


Figure 55. Back-to-Back Diodes Create Settling Issues

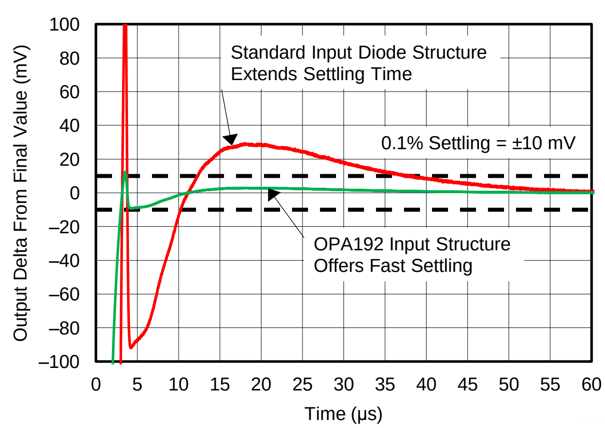


Figure 56. OPA192 Protection Circuit Maintains Fast-Settling Transient Response

Feature Description (continued)

The OPAx192 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPA192 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems; see Figure 66.

8.3.2 EMI Rejection

The OPAx192 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx192 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 57 shows the results of this testing on the OPA192. Table 2 shows the EMIRR IN+ values for the OPA192 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers*, SBOA128, available for download from www.ti.com.

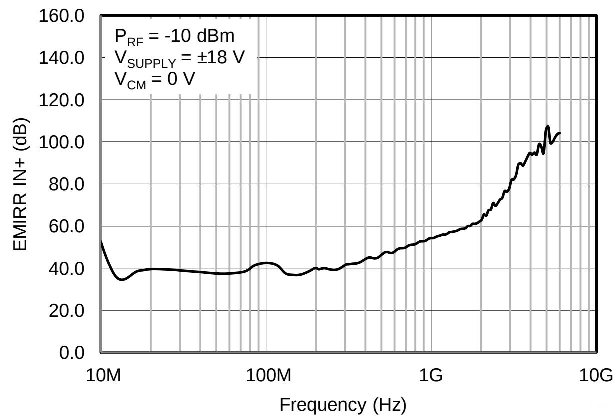


Figure 57. EMIRR Testing

Table 2. OPA192 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

8.3.3 Phase Reversal Protection

The OPAx192 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx192 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 58.

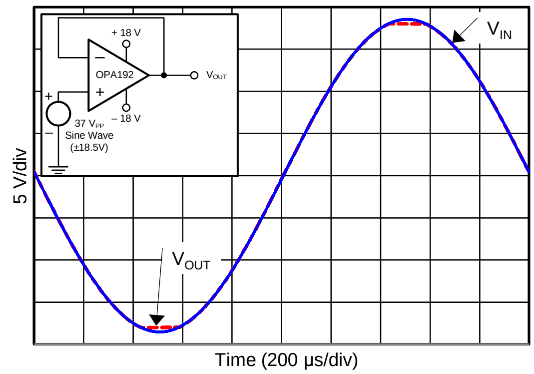


Figure 58. No Phase Reversal

8.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx192 is 150°C. Exceeding this temperature causes damage to the device. The OPAx192 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 59 shows an application example for the OPA192 that has significant self heating (159°C) because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 59 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

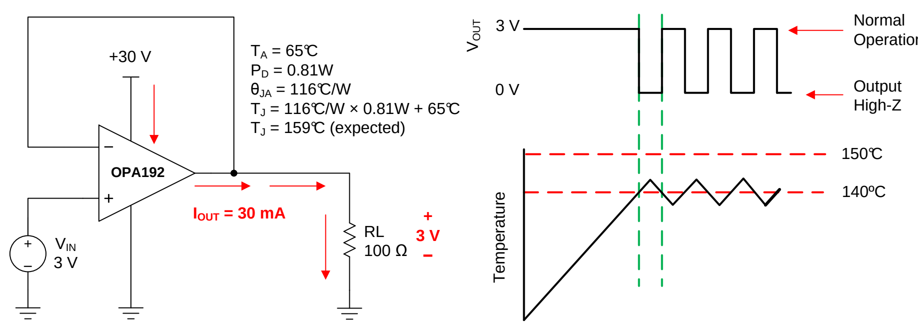


Figure 59. Thermal Protection

8.3.5 Capacitive Load and Stability

The OPAx192 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 60 and Figure 61. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

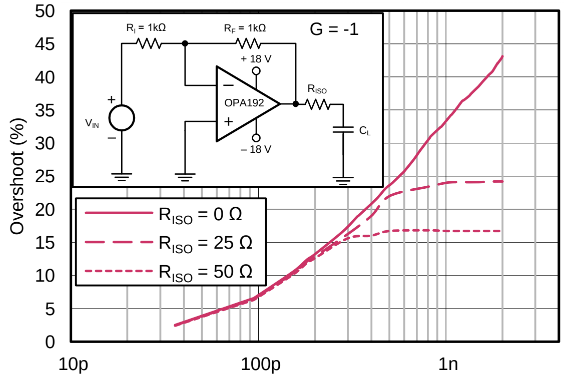


Figure 60. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

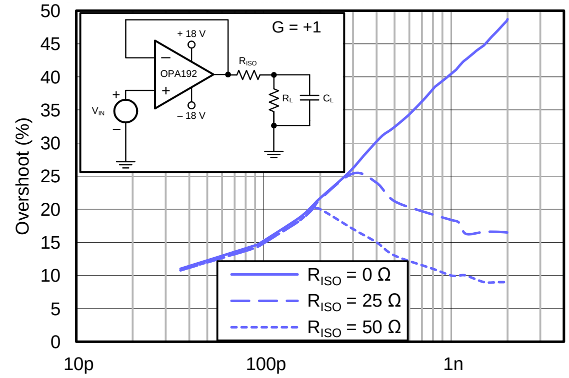


Figure 61. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 62. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPA192 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 62 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and results using the OPA192 are summarized in Table 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

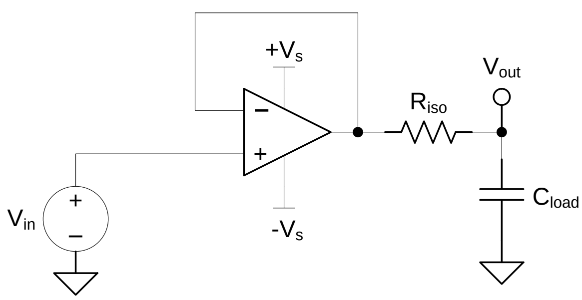


Figure 62. Extending Capacitive Load Drive with the OPA192

Table 3. OPA192 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE									
Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
R_{ISO} (Ω)	47.0	360.0	24.0	100.0	20.0	51.0	6.2	15.8	2.0	4.7
Measured Overshoot (%)	23.2 8.6	10.4	22.5	9.0	22.1	8.7	23.1	8.6	21.0	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* .

8.3.6 Common-Mode Voltage Range

The OPAx192 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 63. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region.

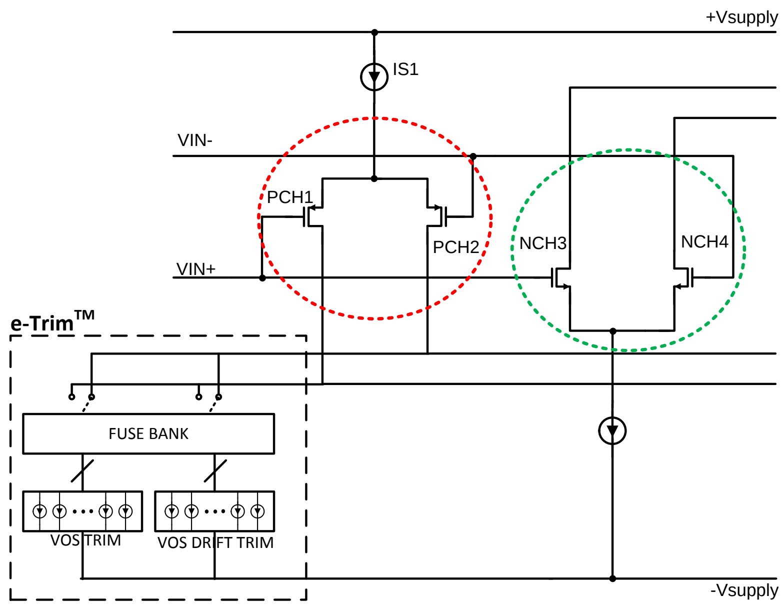


Figure 63. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx192 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 64.

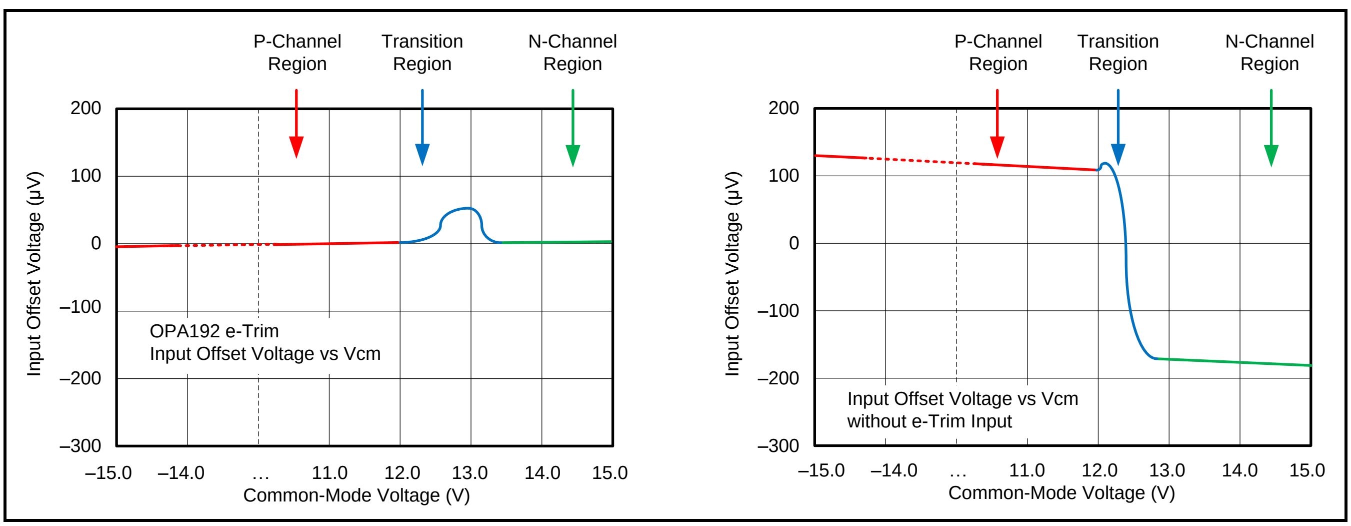


Figure 64. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 65 shows an illustration of the ESD circuits contained in the OPAx192 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

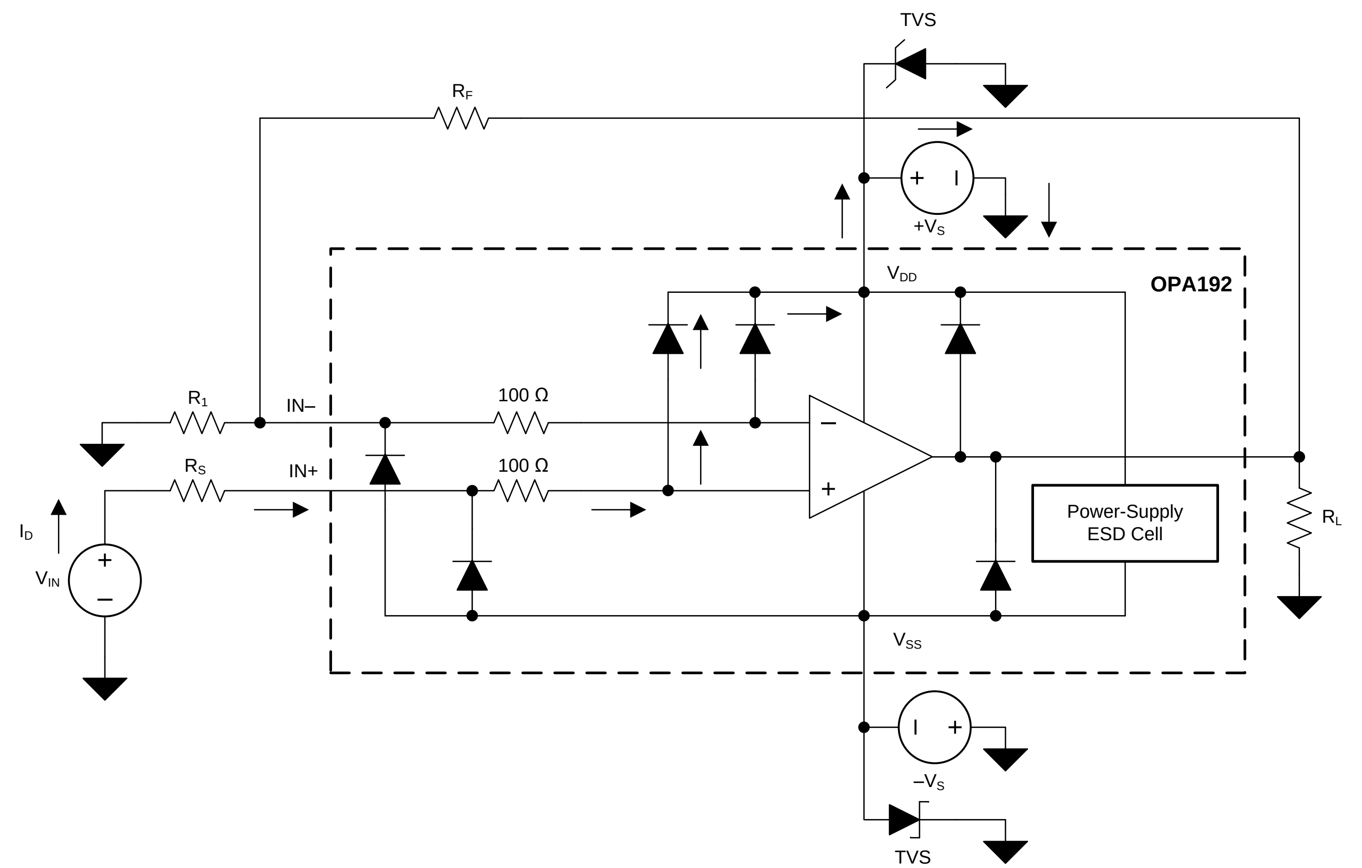


Figure 65. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

8.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx192 is approximately 200 ns.

8.4 Device Functional Modes

The OPAx192 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx192 is 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx192 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input/output, ultralow offset voltage and offset voltage drift, as well as 10-MHz bandwidth and high capacitive load drive. These features make the OPAx192 a robust, high-performance operational amplifier for high-voltage industrial applications.

9.2 Typical Applications

9.2.1 16-Bit Precision Multiplexed Data-Acquisition System

Figure 66 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

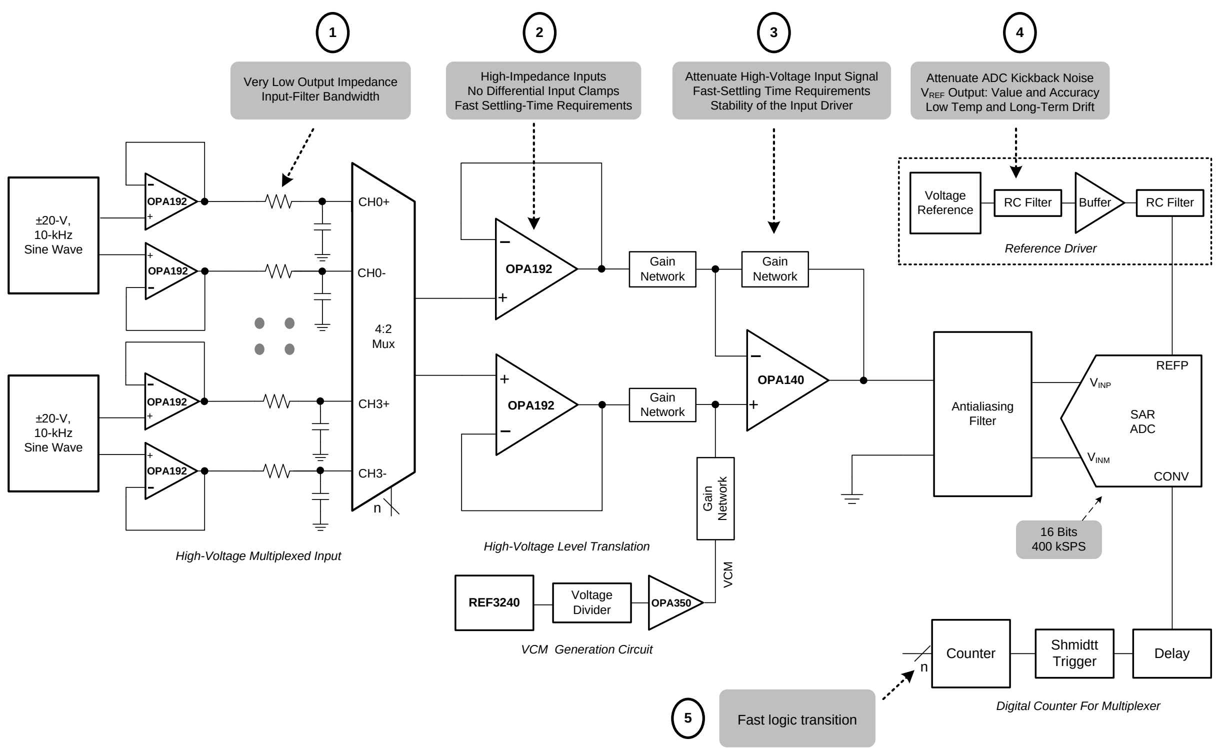


Figure 66. OPA192 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs with Lowest Distortion

9.2.1.1 Design Requirements

The primary objective is to design a ±20 V, differential 4-channel multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10 kHz full-scale pure sine-wave input. The design requirements for this block design are:

Typical Applications (continued)

- System Supply Voltage: ±15 V
- ADC Supply Voltage: 3.3 V
- ADC Sampling Rate: 400 kSPS
- ADC Reference Voltage (REFP): 4.096 V
- System Input Signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

9.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in Figure 66. The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. The diagram includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input when maintaining amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

9.2.1.3 Application Curve

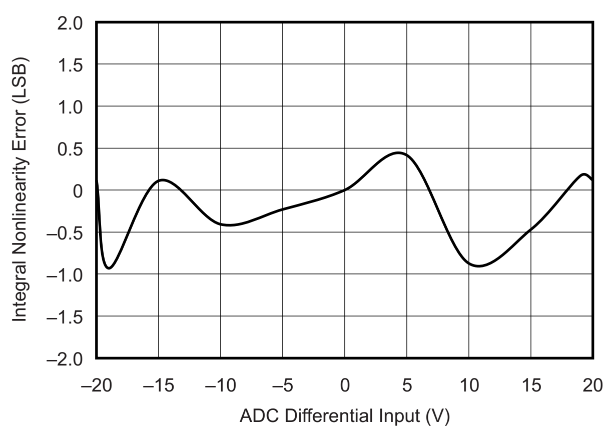


Figure 67. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU181, *16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion*.

9.2.2 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx192 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems.Figure 68 shows the OPA192 in a slew-rate limit design.

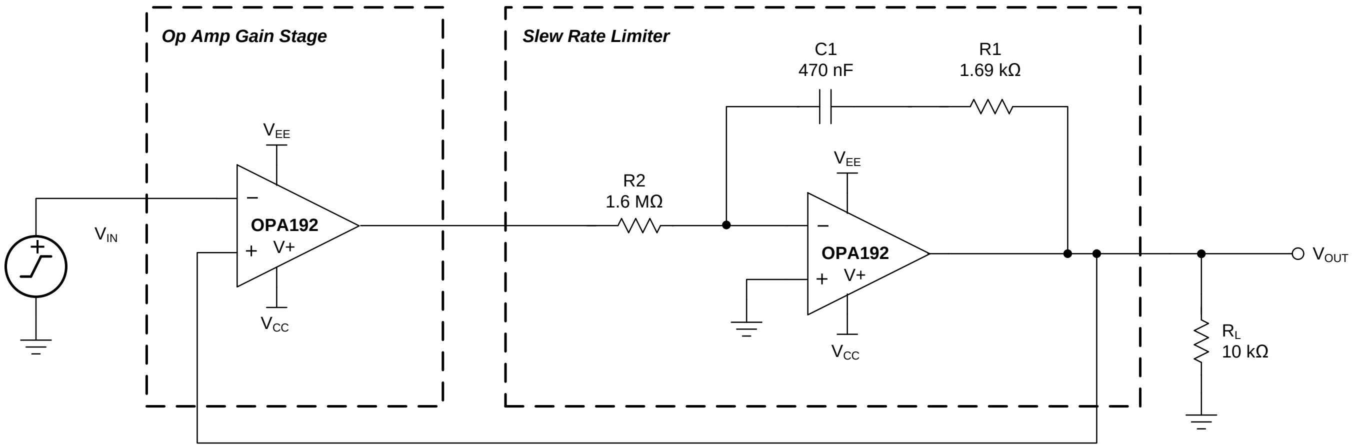


Figure 68. Slew Rate Limiter Uses One Op Amp

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

9.2.3 Precision Reference Buffer

The OPAx192 features high output current drive capability and low input offset voltage, making the device an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10-µF ceramic capacitor shown in Figure 69, R_{ISO}, a 37.4-Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output, V_{OUT}. Feedback path number two is through R_{Fx} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10-µF load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz and still provides a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F, R_{Fx} , C_F , and R_{ISO}.

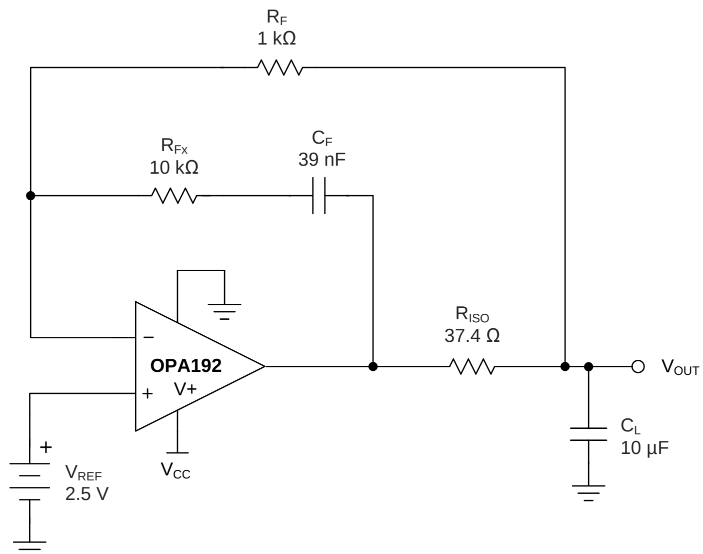


Figure 69. Precision Reference Buffer

10 Power-Supply Recommendations

The OPAx192 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

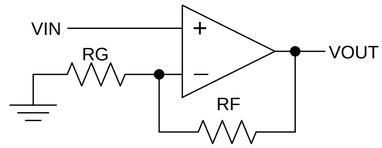
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 70, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example



(Schematic Representation)

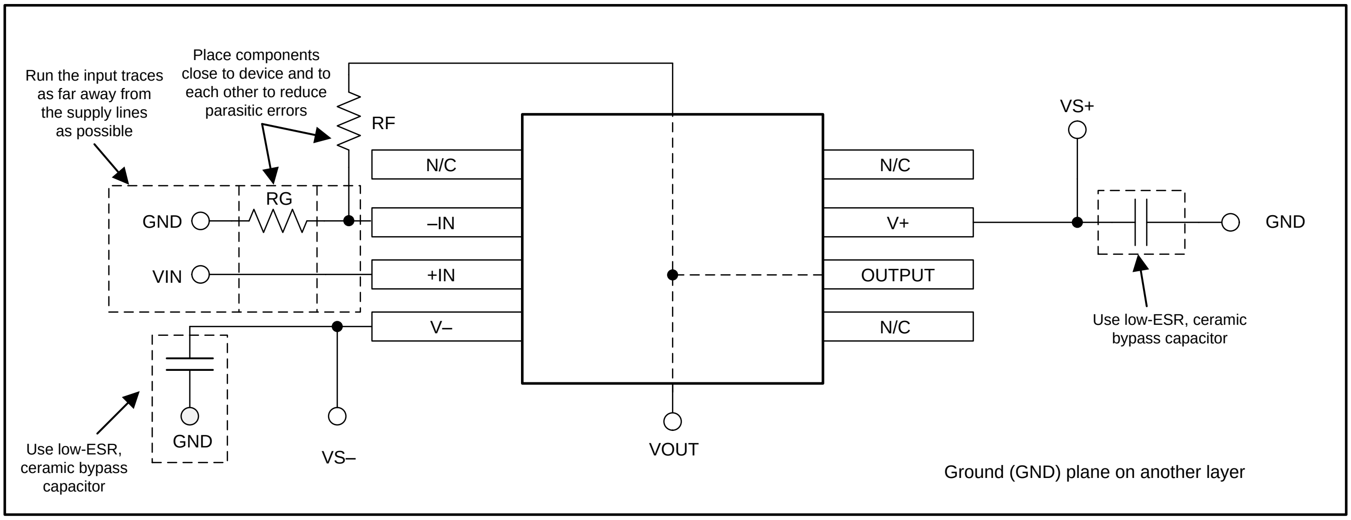


Figure 70. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 TI Precision Designs

The OPA192 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

Circuit Board Layout Techniques, SLOA089.

Op Amps for Everyone, SLOD006.

12.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA192	Click here	Click here	Click here	Click here	Click here
OPA2192	Click here	Click here	Click here	Click here	Click here
OPA4192	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

e-trim, E2E are trademarks of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA192ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA192
OPA192ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA192
OPA192IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS
OPA192IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS
OPA192IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS
OPA192IDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS
OPA192IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS
OPA192IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUYS
OPA192IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS
OPA192IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS
OPA192IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS
OPA192IDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS
OPA192IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS
OPA192IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUXS
OPA192IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA192
OPA192IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA192
OPA192IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA192
OPA192IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA192
OPA2192ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192
OPA2192ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192
OPA2192IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OVLM
OPA2192IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OVLM
OPA2192IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OVLM
OPA2192IDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OVLM
OPA2192IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OVLM
OPA2192IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OVLM
OPA2192IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192
OPA2192IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192
OPA2192IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2192IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2192
OPA4192ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192ID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IDRG4.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	OPA4192
OPA4192IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	OPA4192

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA192, OPA2192 :

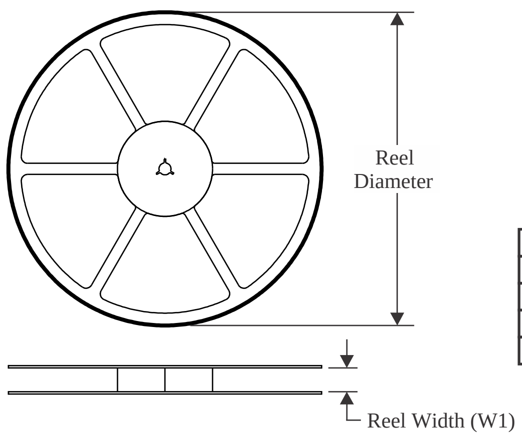
- Automotive : OPA192-Q1, OPA2192-Q1

NOTE: Qualified Version Definitions:

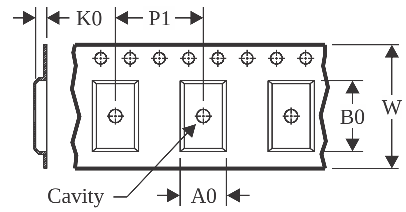
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

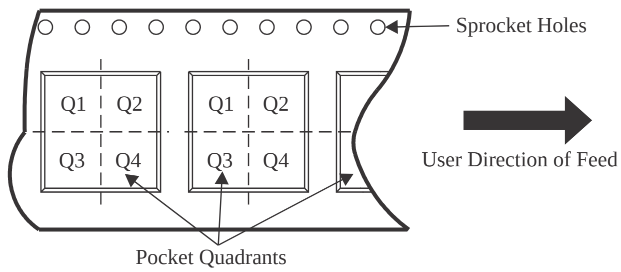


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

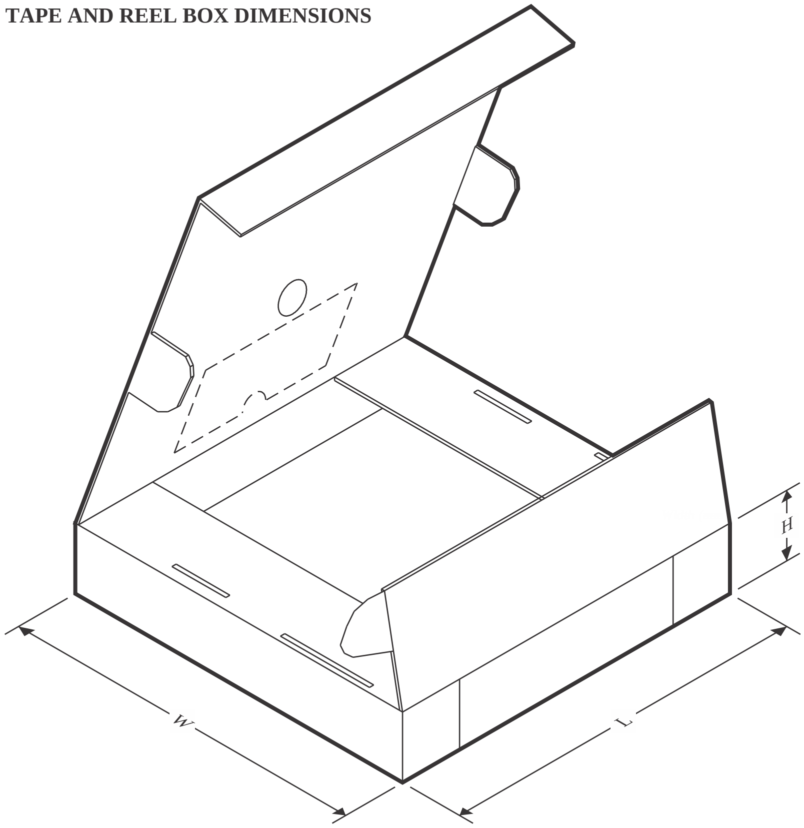
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA192IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA192IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA192IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA192IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA192IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA192IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA192IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA192IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2192IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2192IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2192IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2192IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2192IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4192IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4192IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4192IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

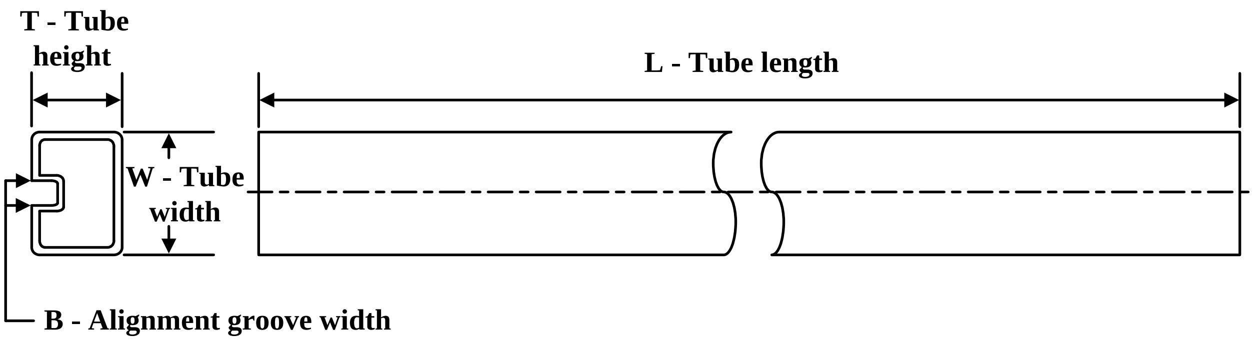
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

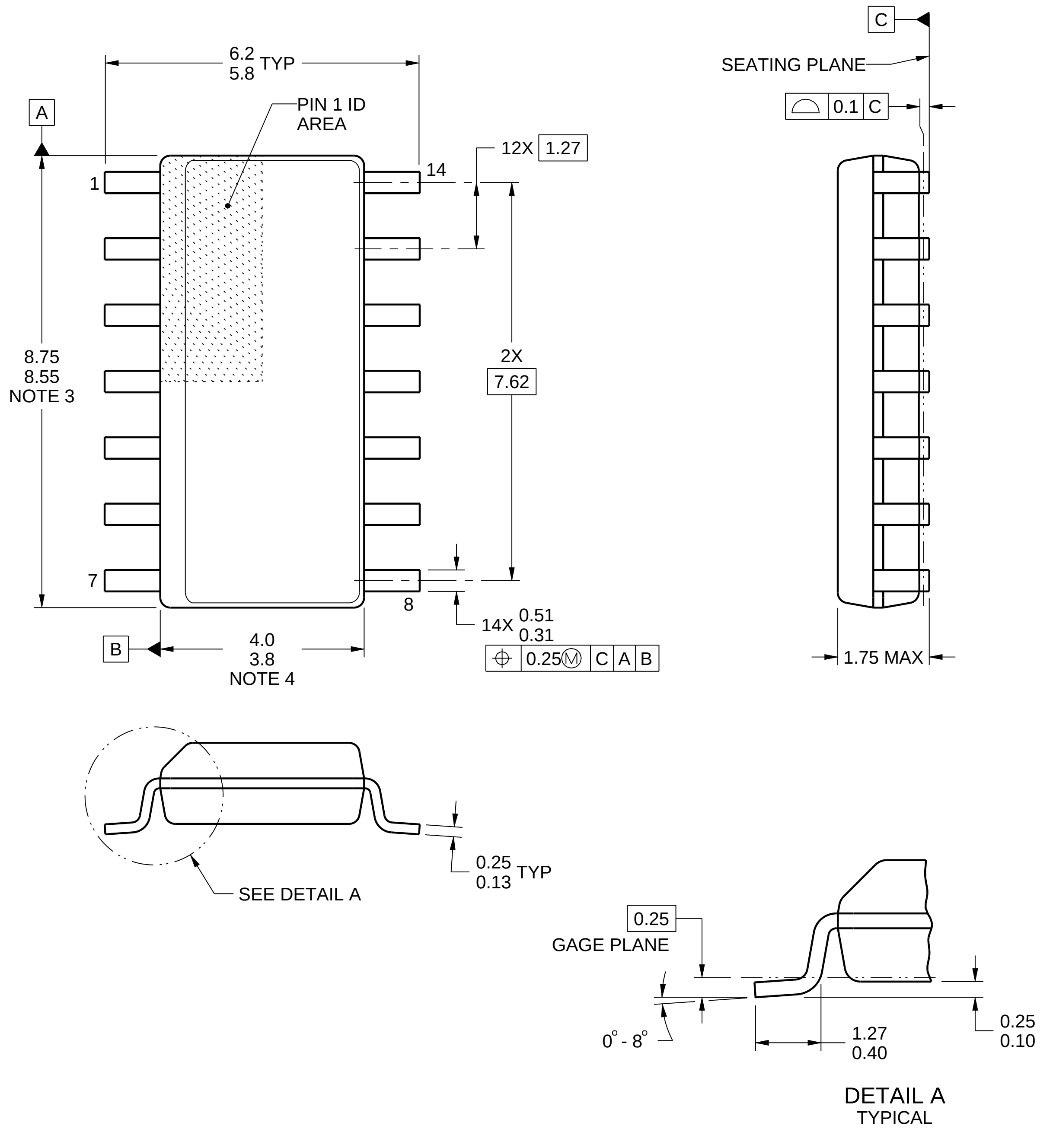
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA192IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA192IDBVRG4	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA192IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA192IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
OPA192IDGKRG4	VSSOP	DGK	8	2500	358.0	335.0	35.0
OPA192IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA192IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA192IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA2192IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA2192IDGKRG4	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA2192IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA2192IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2192IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA4192IDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4192IDRG4	SOIC	D	14	2500	353.0	353.0	32.0
OPA4192IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

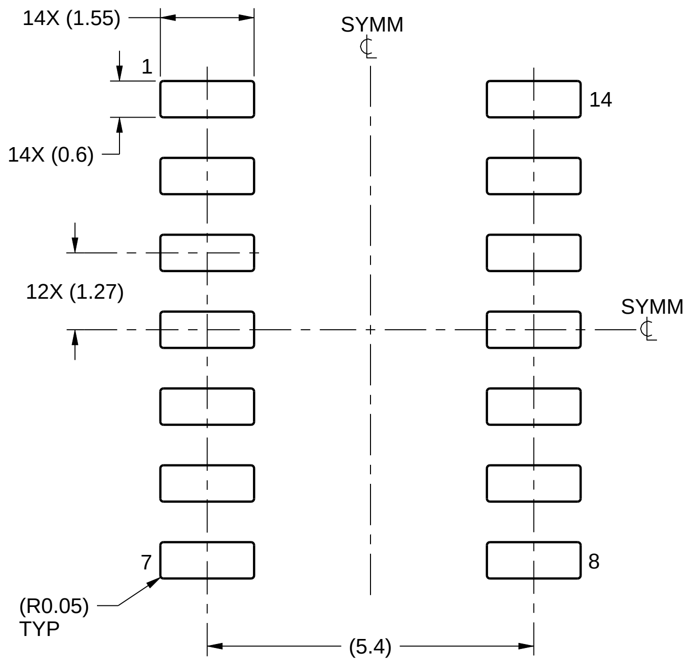
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA192ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA192ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2192ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2192ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4192ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4192ID.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4192IPW	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4192IPW.B	PW	TSSOP	14	90	508	8.5	3250	2.8



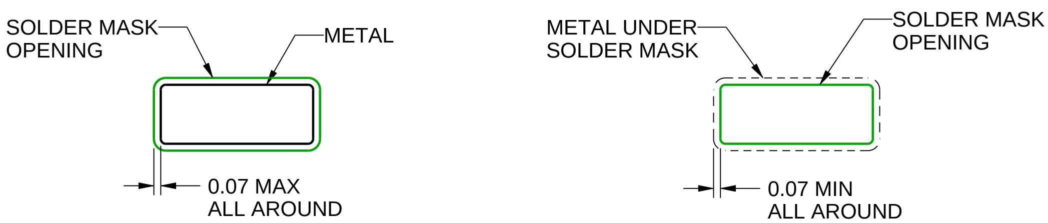
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



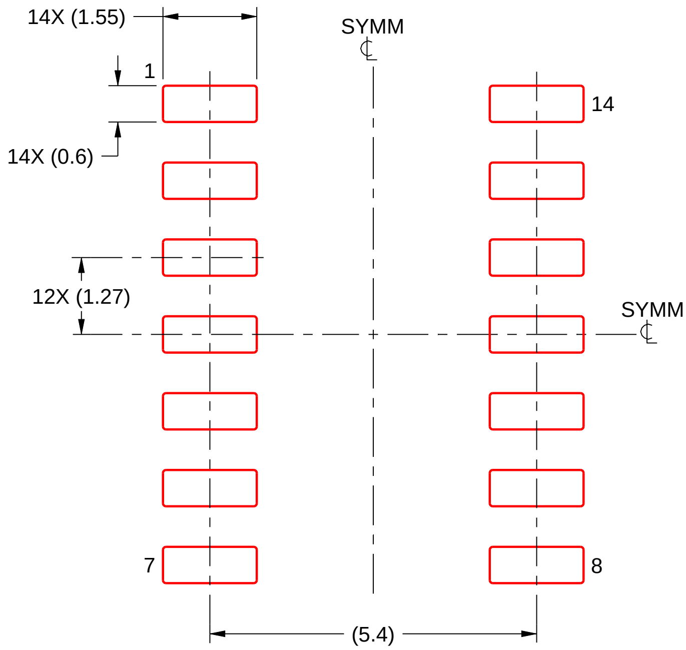
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

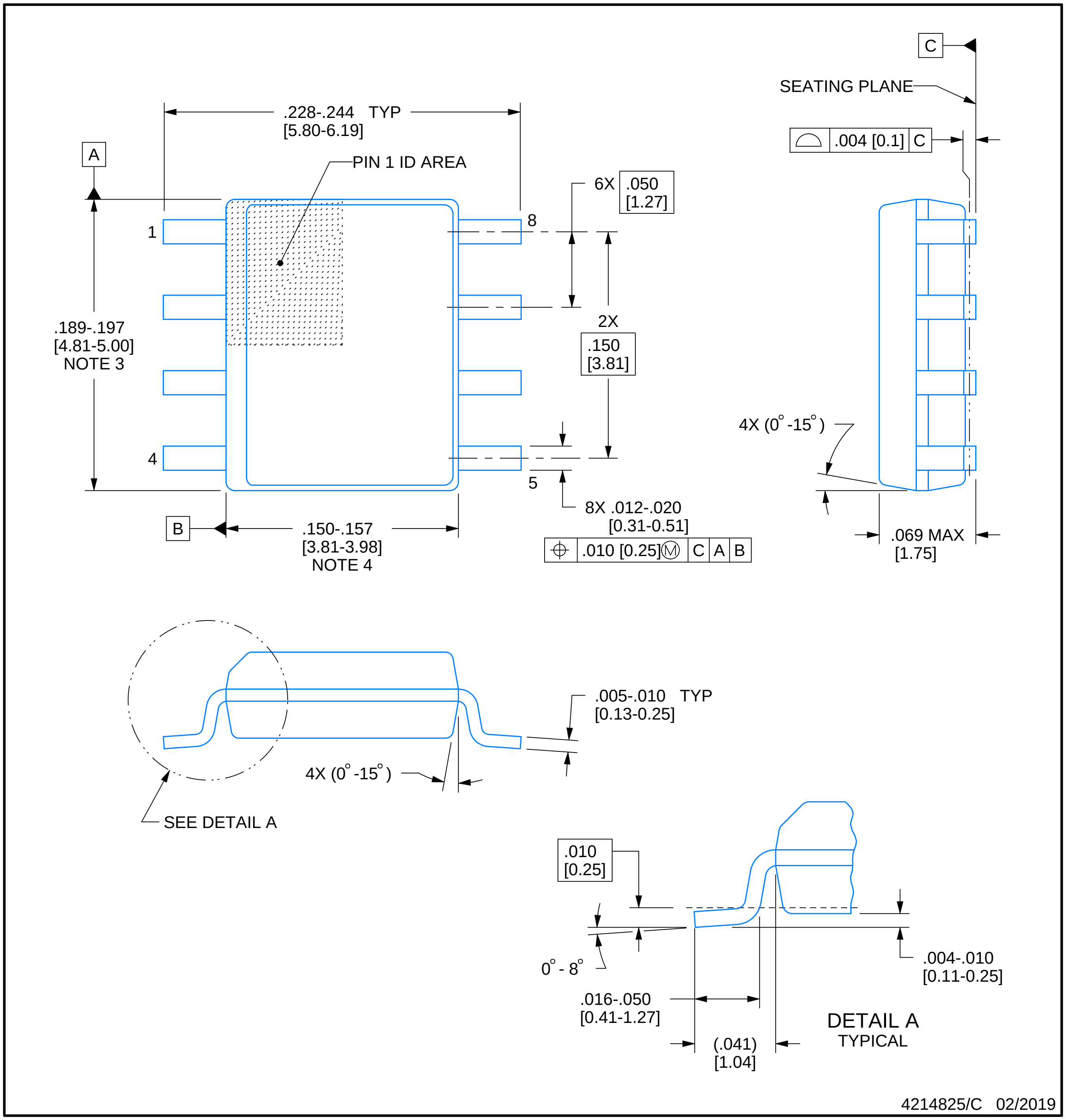


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

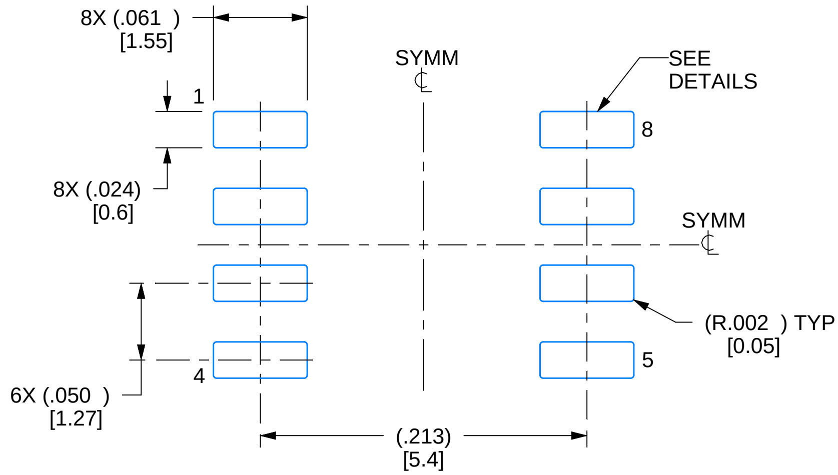
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

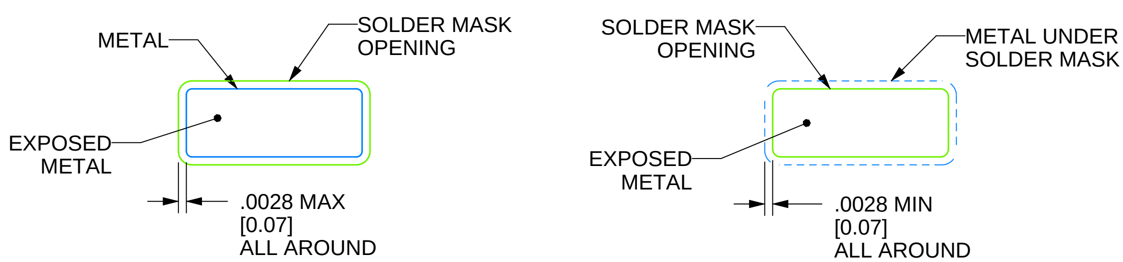


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

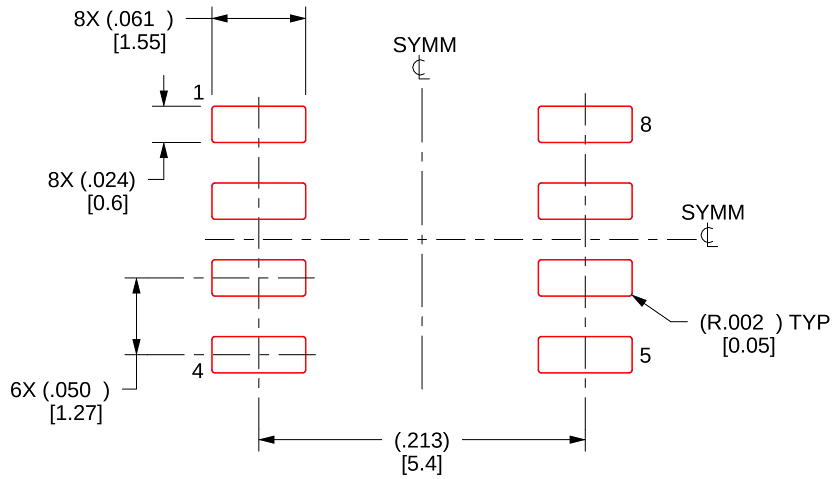
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

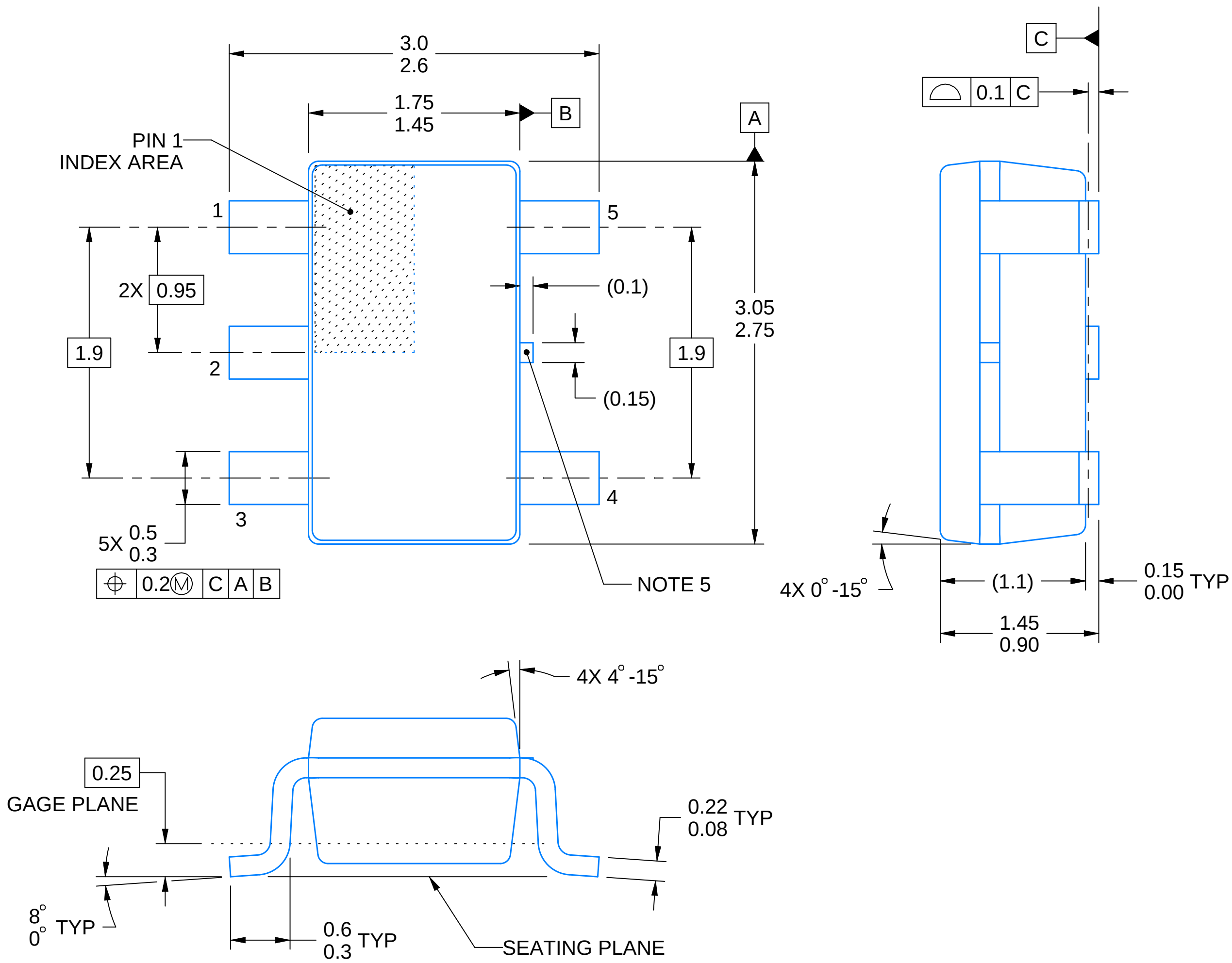


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

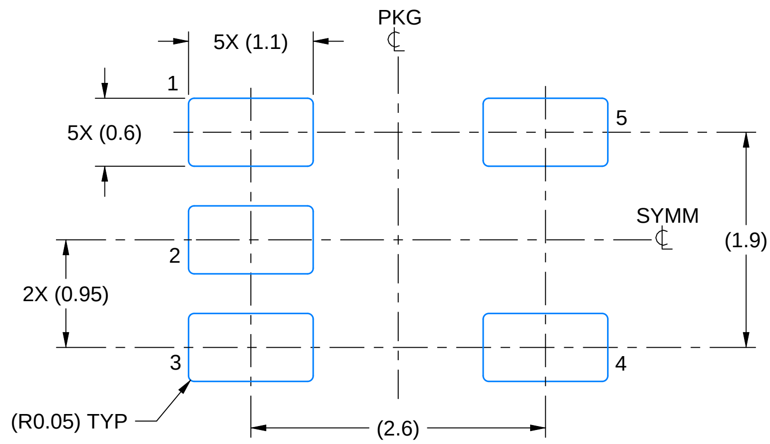
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



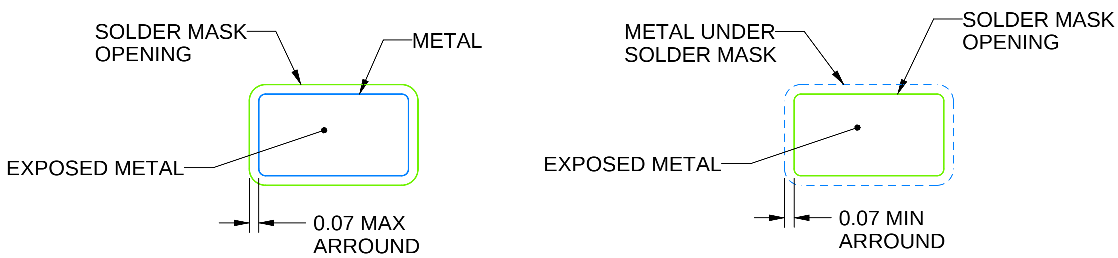
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

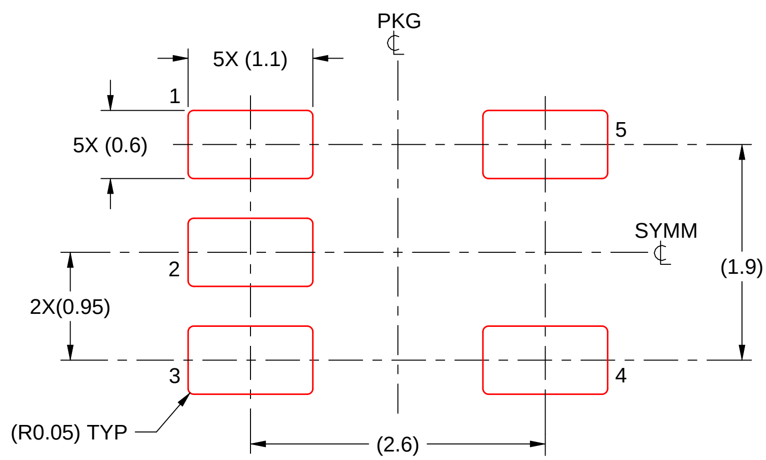
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

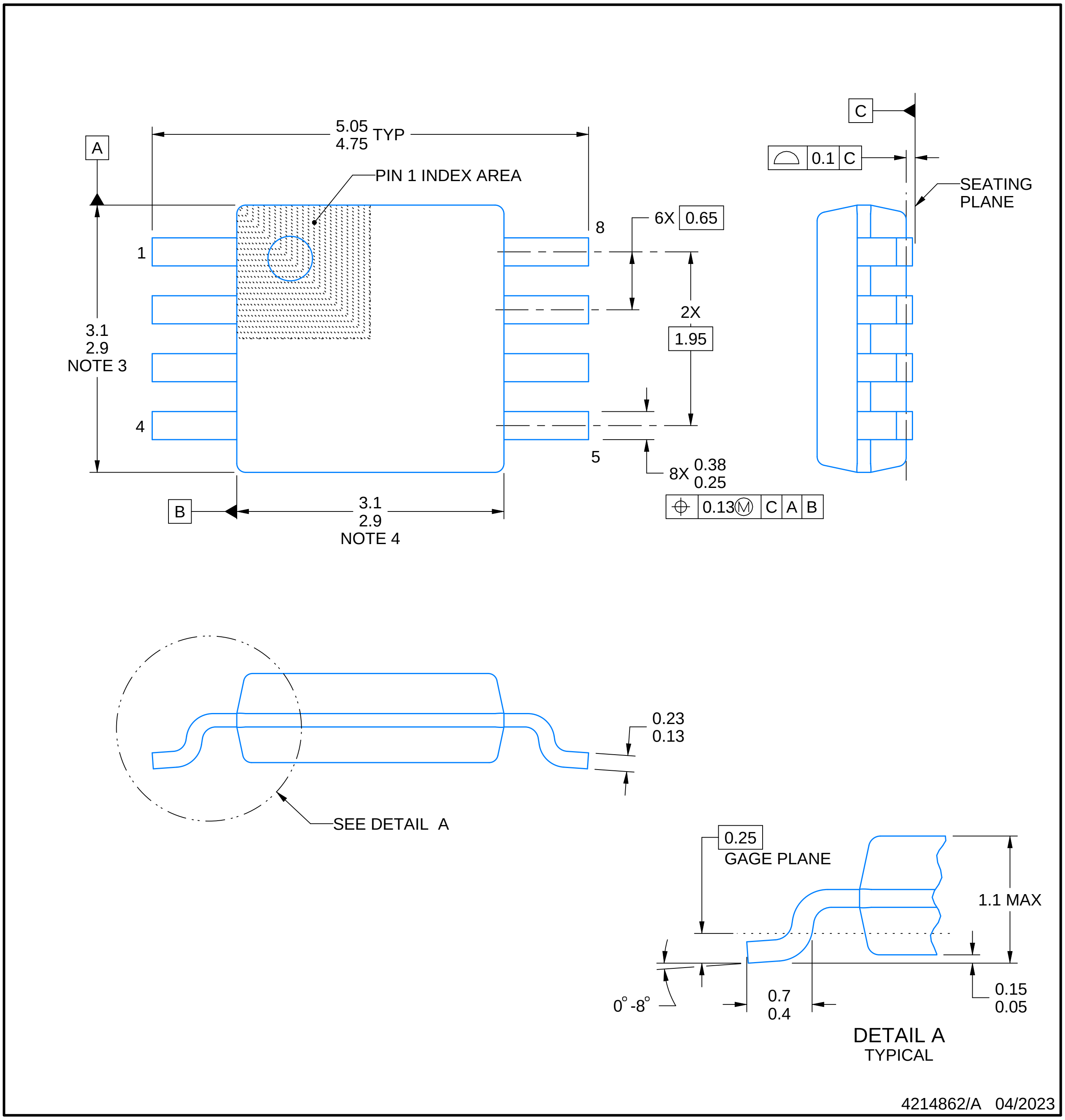


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

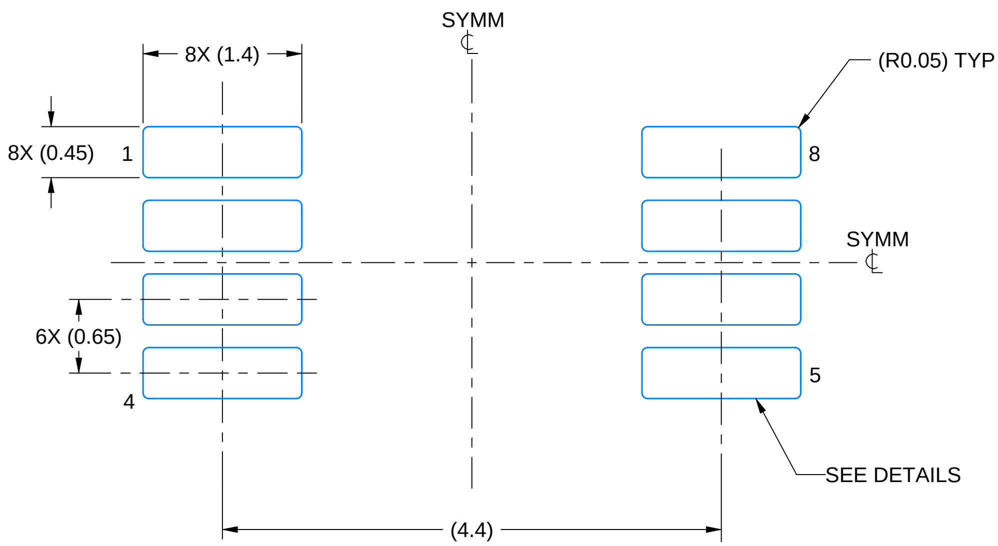
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



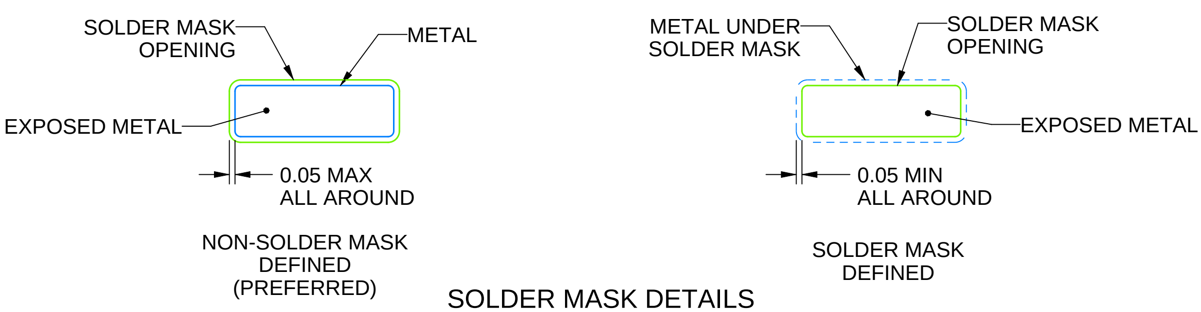
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

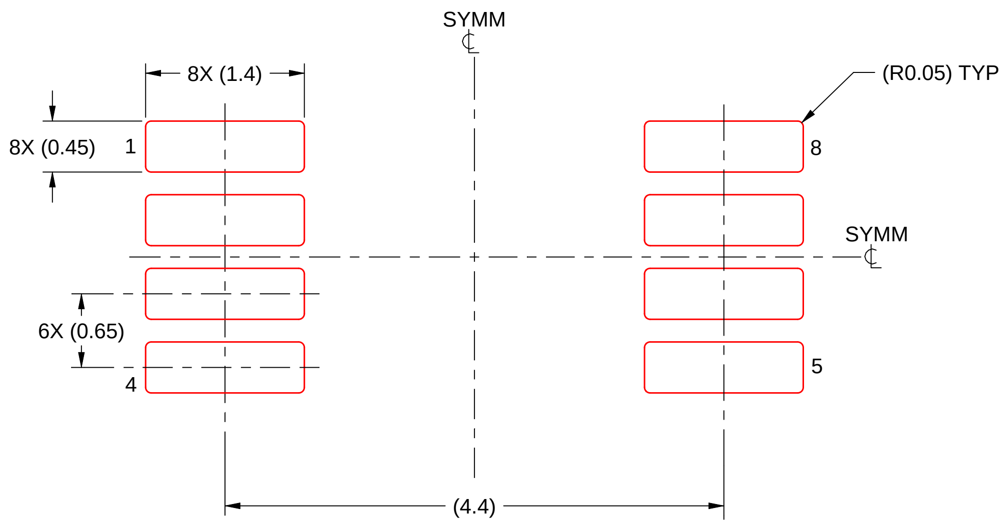


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

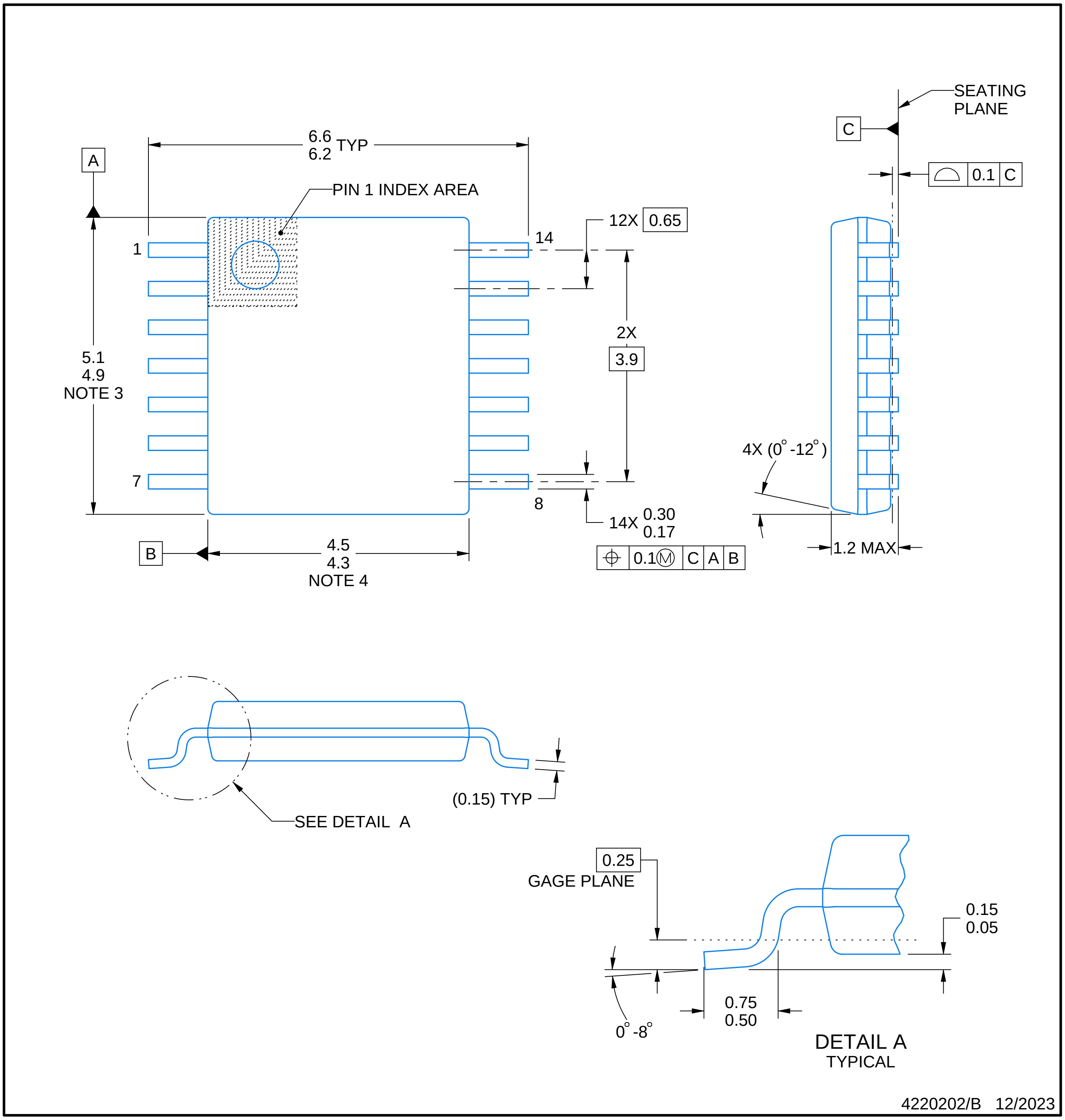


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

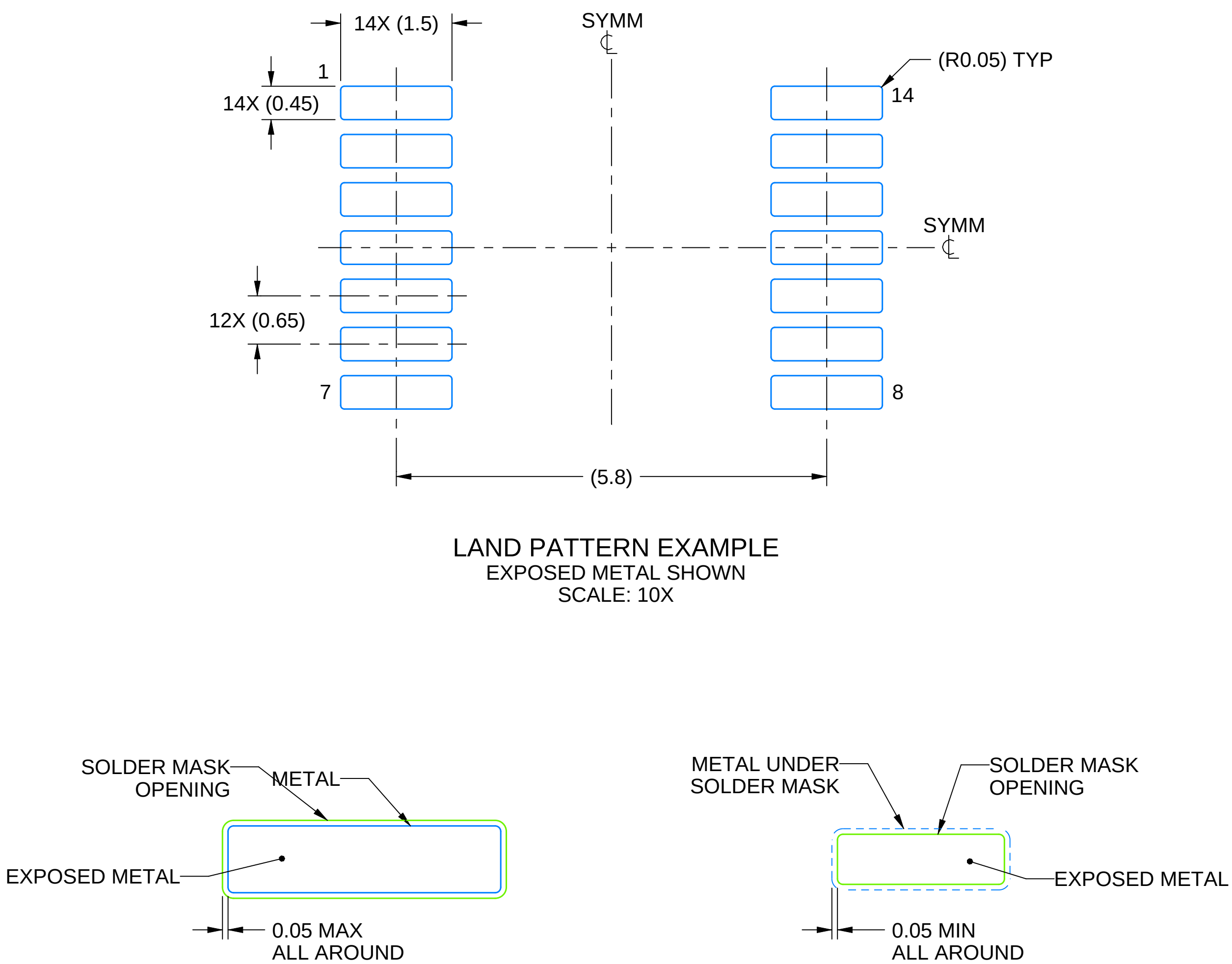
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

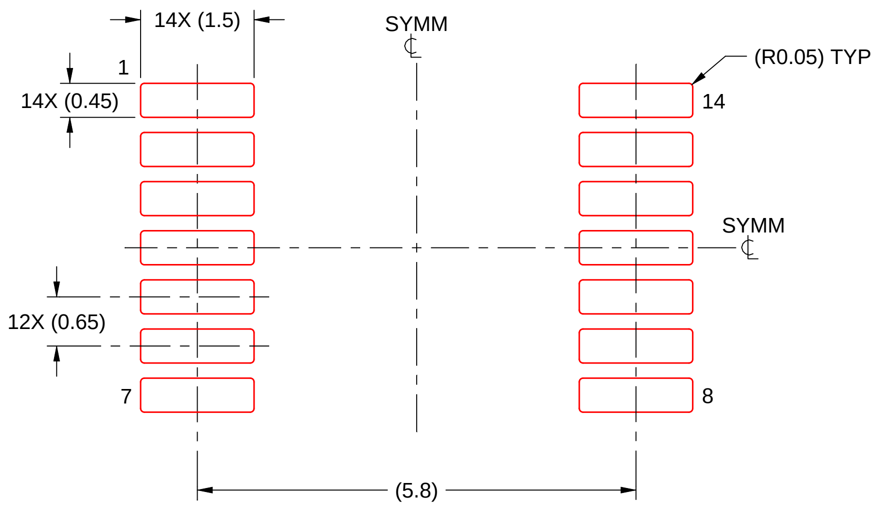
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.