TL5209 500-mA Low-Noise Low-Dropout Voltage Regulator With Shutdown

1 Features

- Adjustable Output Voltage
- 1%/2% Accuracy (25°C/Full Range)
- 500-mV (Maximum) Dropout at Full Load of 500 mA
- Tight Regulation Overtemperature Range
  - 0.1%/V (Maximum) Line Regulation
  - 0.7% (Maximum) Load Regulation
- Ultra Low-Noise Capability (300 nV/$\sqrt{\text{Hz}}$ Typical)
- Shutdown Current of 3 µA (Maximum)
- Low Temperature Coefficient
- Current Limiting and Thermal Protection
- Stable With Minimum Load of 1 mA
- Reverse-Battery Protection
- Applications
  - Portable Applications (PDAs, Laptops, Cell Phones)
  - Consumer Electronics
  - Post-Regulation for SMPS
- Available in Convenient SOIC-8 Surface-Mount Package

2 Applications

- Set-Top Boxes
- PCs and Notebooks
- EPOS
- Building Automation

3 Description

The TL5209 device is 500-mA low-dropout (LDO) regulator that is well suited for portable applications. It has a lower quiescent current than most traditional PNP regulators and allows for a shutdown current of 0.05 µA (typical). The TL5209 also has very good dropout voltage characteristics, requiring a maximum dropout of 10 mV at light loads and 500 mV at full load. In addition, the LDO also has a 1% output voltage accuracy and very tight line and load regulation that is comparable to its CMOS counterparts.

For noise-sensitive applications, the TL5209 allows for low-noise capability through an external bypass capacitor connected to the BYP pin, which reduces the output noise of the regulator. Other features include current limiting, thermal shutdown, reverse-battery protection, and low temperature coefficient.

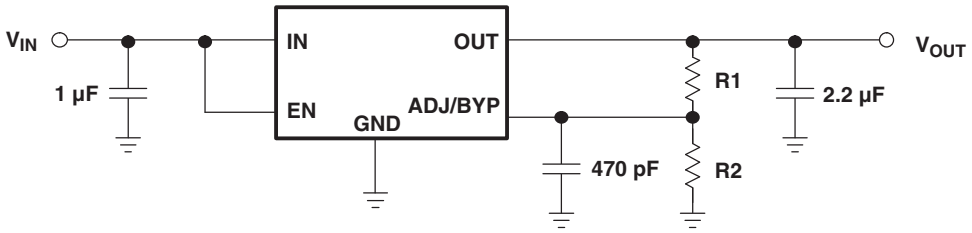
The TL5209 is available with adjustable output. Offered in an SOIC-8 surface-mount package, the TL5209 is characterized for operation over the virtual junction temperature ranges of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL5209	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Schematic



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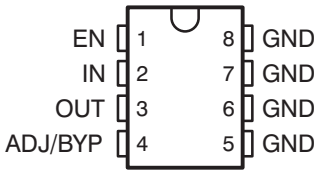
5 Revision History

Changes from Revision A (May 2007) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ/BYP	4	I	Adjust/Bypass pin, forces a constant voltage of 1.242 V to allow for adjusting the output voltage with external resistors. A bypass capacitance can be used on this pin to slow down the ramp up of the output voltage.
EN	1	I	Control input, active high
GND	5-8	-	Ground
IN	2	I	Input voltage
OUT	3	O	Output voltage

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Continuous input voltage	–20	20	V
V_O	Output voltage		7.5	V
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	Input voltage	2.5	16	V
V_O	Output voltage		6.5	V
V_{EN}	Enable input voltage	0	V_I	V
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TL5209 D [SOIC] 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

$V_{IN} = V_{OUT} + 1$ V, $C_{OUT} = 4.7$ µF, $I_{OUT} = 1$ mA, full range $T_J = –40°C$ to 125°C

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
	Output voltage accuracy	V_{OUT} = 2.5 V for ADJ only	25°C	–1%		1%	
			–40°C to 125°C	–2%		2%	
αV_{OUT}	Output voltage temperature coefficient		–40°C to 125°C		40		ppm/°C
	Line regulation	V_{IN} = (V_{OUT} + 1 V) to 16 V	25°C		0.009	0.05	%/V
			–40°C to 125°C			0.1	
	Load regulation	I_{OUT} = 1 mA to 500 mA[1]	25°C		0.05%	0.5%	
			–40°C to 125°C			0.7%	
$V_{IN} – V_{OUT}$	Dropout voltage[2]	I_{OUT} = 1 mA	25°C		45	60	mV
			–40°C to 125°C			80	
		I_{OUT} = 50 mA	25°C		115	175	
			–40°C to 125°C			250	
		I_{OUT} = 100 mA	25°C		150	250	
			–40°C to 125°C			300	
		I_{OUT} = 500 mA	25°C		350	500	
			–40°C to 125°C			600	
I_Q	Quiescent current	$V_{EN} \geq 3$ V, I_{OUT} = 1 mA	25°C		100	140	µA
			–40°C to 125°C			170	
		$V_{EN} \geq 3$ V, I_{OUT} = 50 mA	25°C		350	650	
			–40°C to 125°C			900	
		$V_{EN} \geq 3$ V, I_{OUT} = 100 mA	25°C		1.2	2	mA
			–40°C to 125°C			3	
		$V_{EN} \geq 3$ V, I_{OUT} = 500 mA	25°C		8	20	
			–40°C to 125°C			25	
I_{min}	Minimum load current[3]		–40°C to 125°C			1	mA
I_{SD}	Shutdown current	$V_{EN} \leq 0.4$ V	25°C		0.05	3	µA
		$V_{EN} \leq 0.18$ V	25°C		0.1		
			–40°C to 125°C			8	
	Ripple rejection	f = 120 Hz	25°C		75		dB
I_{LIMIT}	Current limit	V_{OUT} = 0 V	25°C		700	900	mA
			–40°C to 125°C			1000	

(1) Low duty cycle testing is used to maintain the junction temperature as close to the ambient temperature as possible. Changes in output voltage due to thermal effects are covered separately by the thermal regulation specification.
(2) Dropout is defined as the input to output differential at which the output drops 2% below its nominal value measured at 1-V differential.
(3) For stability across the input voltage and temperature. For ADJ versions, the minimum current can be set by R1 and R2.

Electrical Characteristics (continued)

V_{IN} = V_{OUT} + 1 V, C_{OUT} = 4.7 µF, I_{OUT} = 1 mA, full range T_J = –40°C to 125°C

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
$\Delta V_{OUT}/\Delta P_D$	Thermal regulation(4)	V_{IN} = 16 V, 500-mA load pulse for t = 10 ms	25°C		0.05		%/W
V_n	Output noise	V_{OUT} = 2.5 V, I_{OUT} = 50 mA, C_{OUT} = 2.2 µF, C_{BYP} = 0	25°C		500		nV/√Hz
		I_{OUT} = 50 mA, C_{OUT} = 2.2 µF, C_{BYP} = 470 pF(5)	25°C		300		
V_{EN}	Enable logic voltage	V_{EN} = logic LOW (shutdown)	25°C			0.4	V
			–40°C to 125°C			0.18	
		V_{EN} = logic HIGH (enabled)	25°C	2			
I_{EN}	Enable input current	V_{EN} ≤ 0.4 V (shutdown)	25°C		0.01	–1	µA
		V_{EN} ≤ 0.18 V (shutdown)	–40°C to 125°C		0.01	–2	
		V_{EN} ≥ 2 V (enabled)	25°C		5	20	
			–40°C to 125°C			25	

(4) Thermal regulation is defined as the change in output voltage at a specified time after a change in power dissipation is applied, excluding line and load regulation effects.
(5) C_{BYP} is optional and connected to the BYP/ADJ pin.

7.6 Typical Characteristics

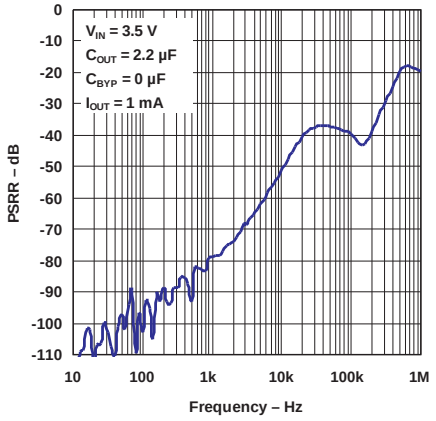


Figure 1. Power Supply Rejection Ratio

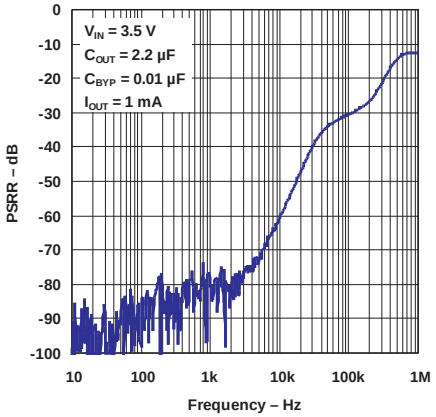


Figure 2. Power Supply Rejection Ratio

Typical Characteristics (continued)

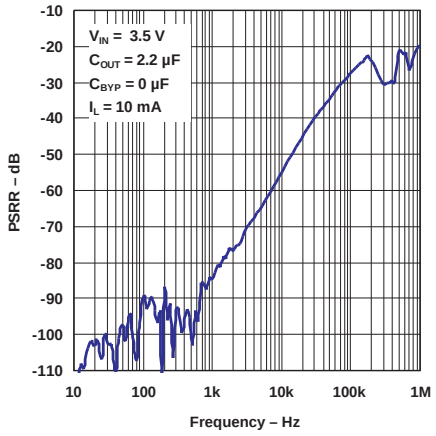


Figure 3. Power Supply Rejection Ratio

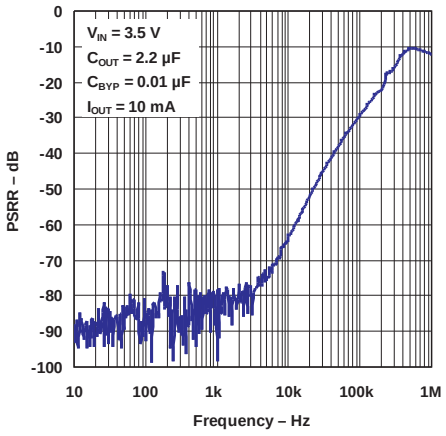


Figure 4. Power Supply Rejection Ratio

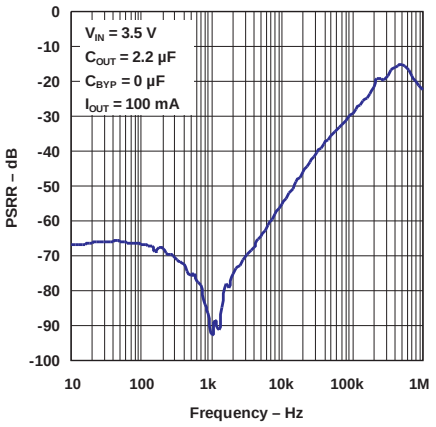


Figure 5. Power Supply Rejection Ratio

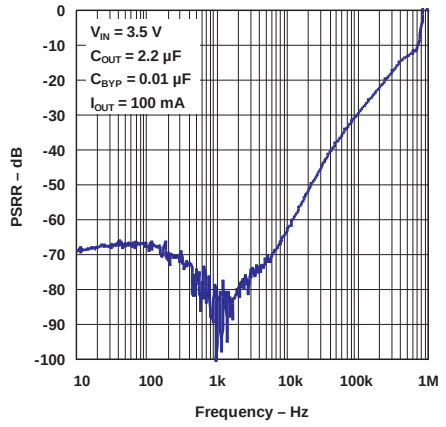


Figure 6. Power Supply Rejection Ratio

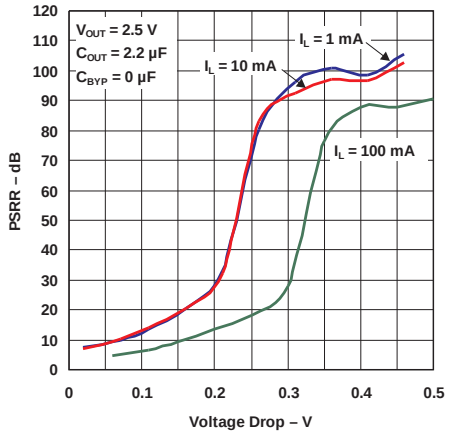


Figure 7. Power Supply Ripple Rejection vs Voltage Drop

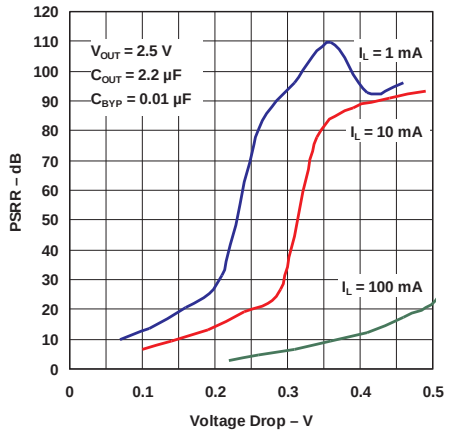


Figure 8. Power Supply Ripple Rejection vs Voltage Drop

Typical Characteristics (continued)

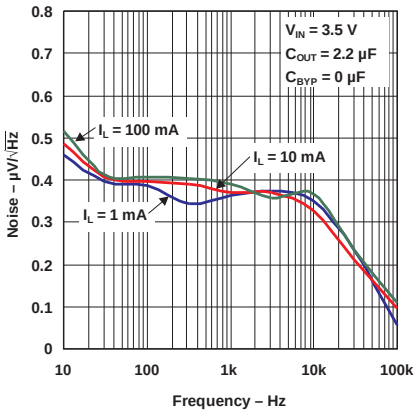


Figure 9. Noise Performance

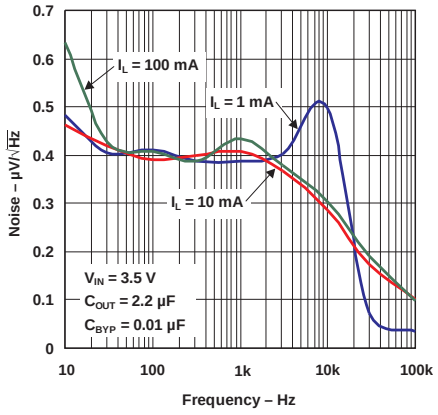


Figure 10. Noise Performance

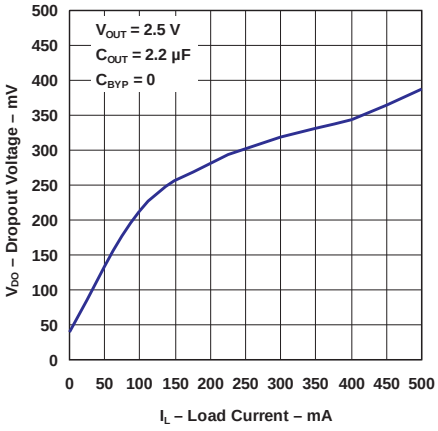


Figure 11. Dropout Voltage vs Load Current

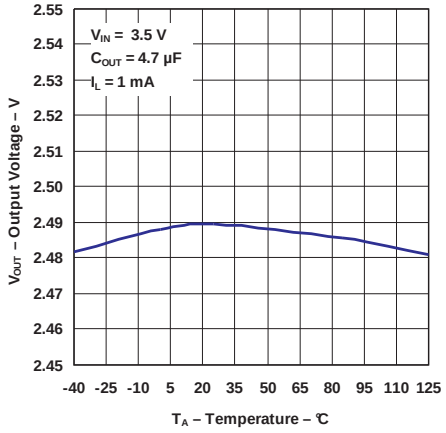


Figure 12. Output Voltage vs Temperature

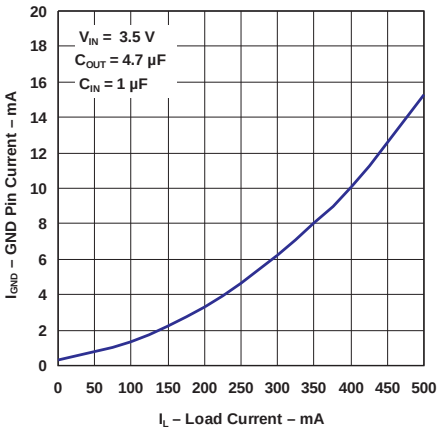


Figure 13. Ground Current vs Load Current

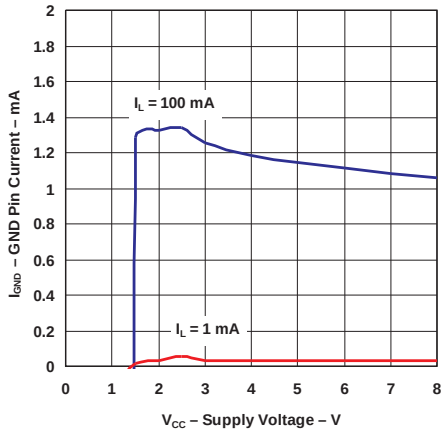


Figure 14. Ground Current vs Supply Voltage

Typical Characteristics (continued)

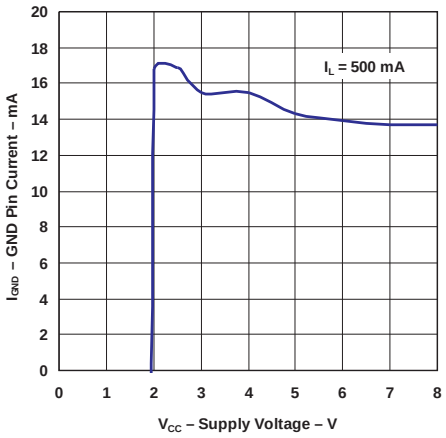


Figure 15. Ground Current vs Supply Voltage

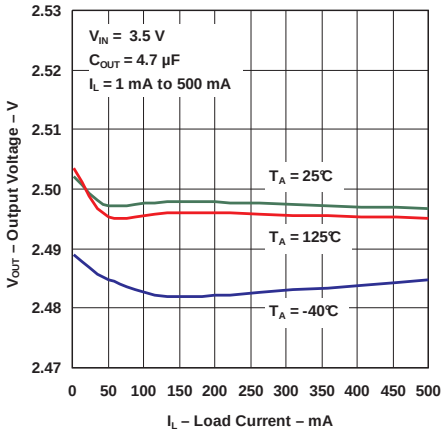


Figure 16. Output Voltage vs Load Current

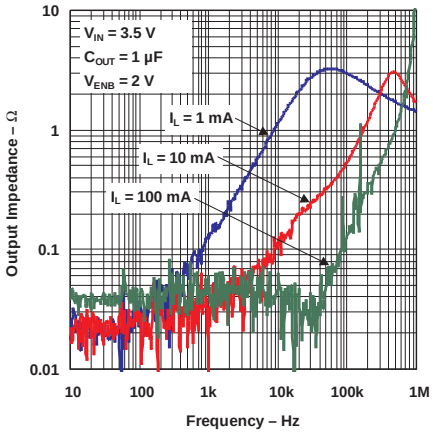


Figure 17. Output Impedance vs Frequency

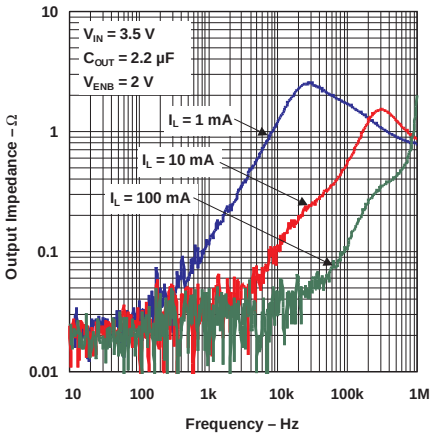


Figure 18. Output Impedance vs Frequency

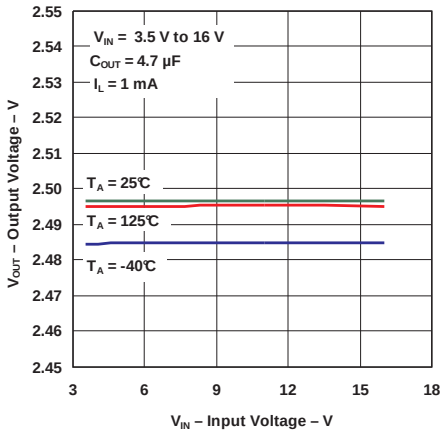


Figure 19. Output Voltage vs Input Voltage

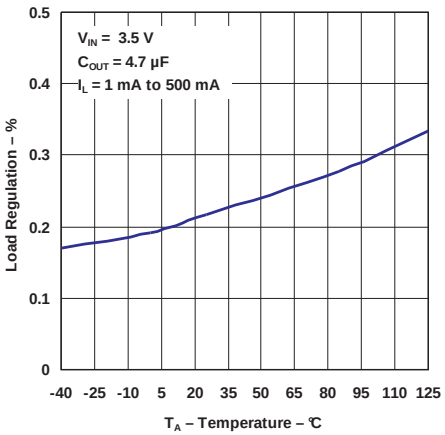


Figure 20. Load Regulation

Typical Characteristics (continued)

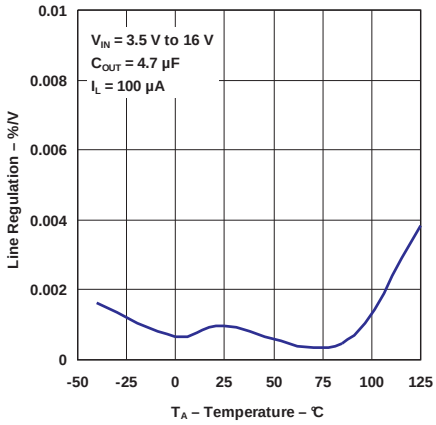


Figure 21. Line Regulation

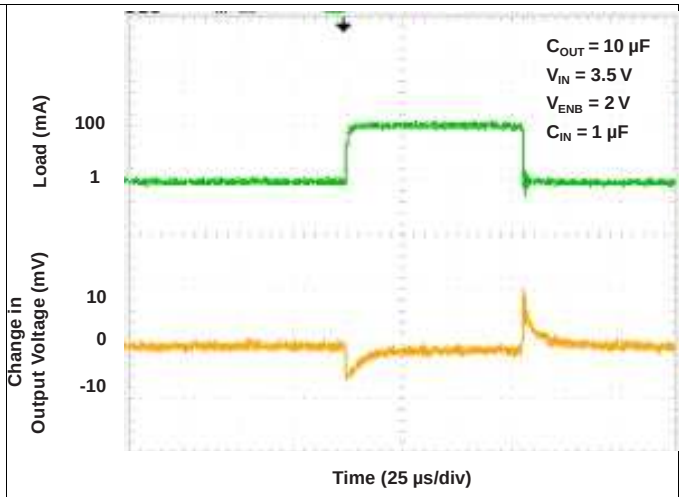


Figure 22. Load Transient Response

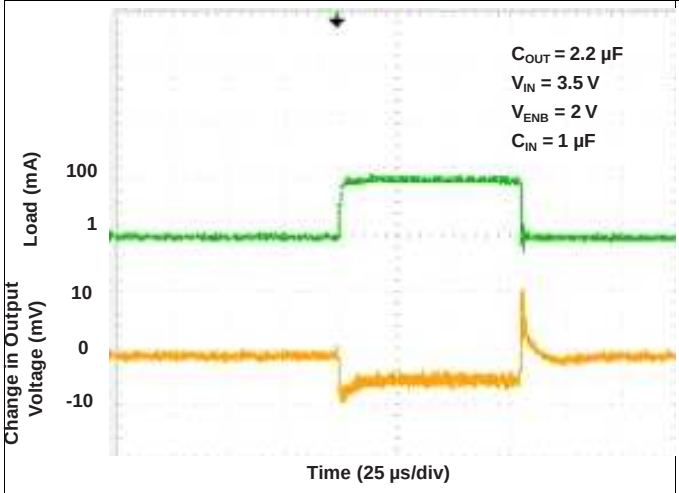


Figure 23. Load Transient Response

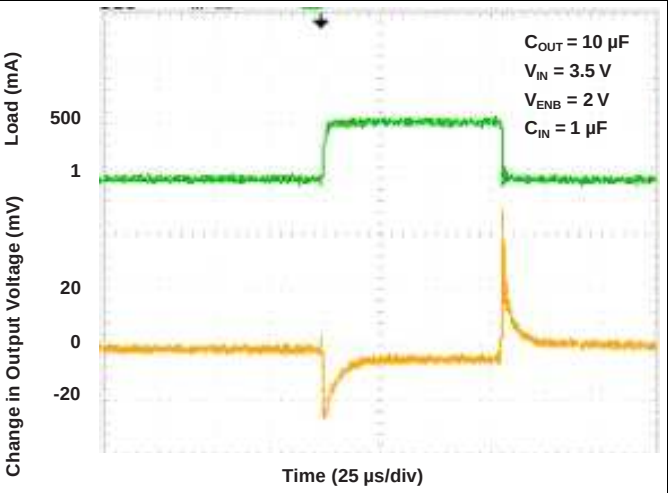


Figure 24. Load Transient Response

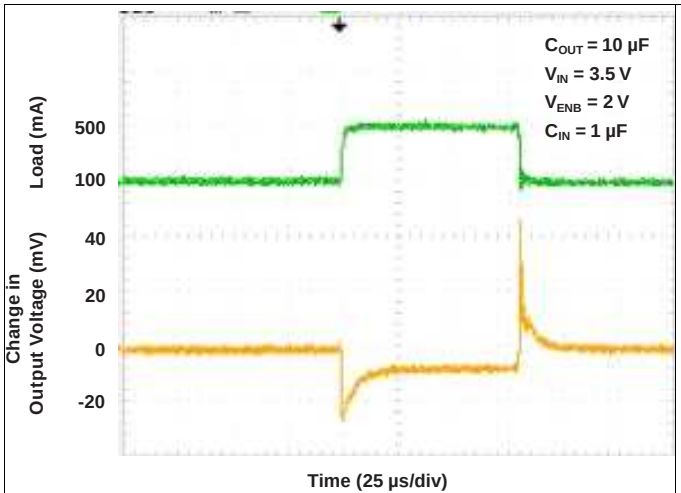


Figure 25. Load Transient Response

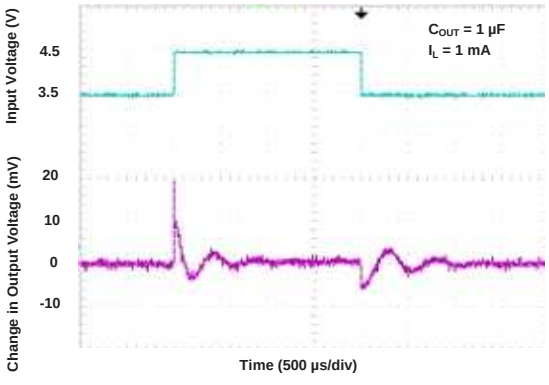


Figure 26. Line Transient Response

Typical Characteristics (continued)

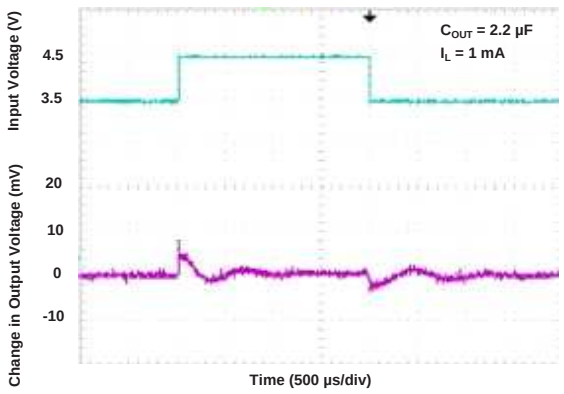


Figure 27. Line Transient Response

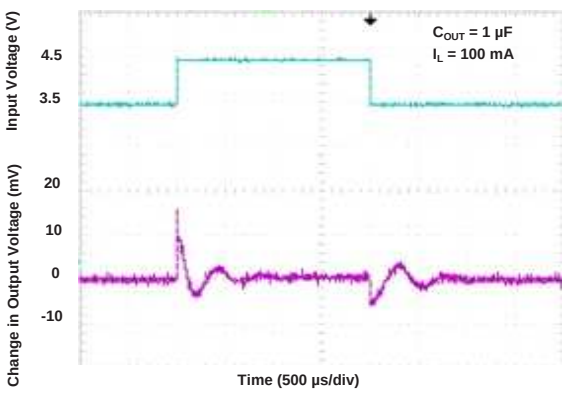


Figure 28. Line Transient Response

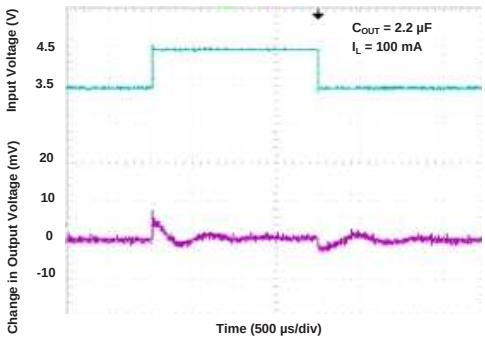


Figure 29. Line Transient Response

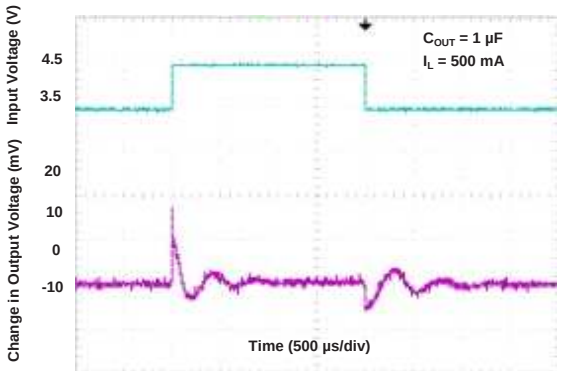


Figure 30. Line Transient Response

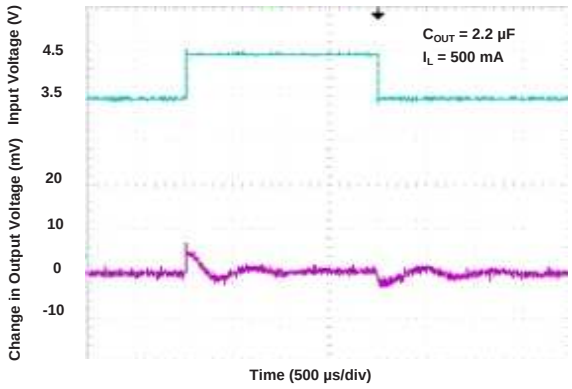


Figure 31. Line Transient Response

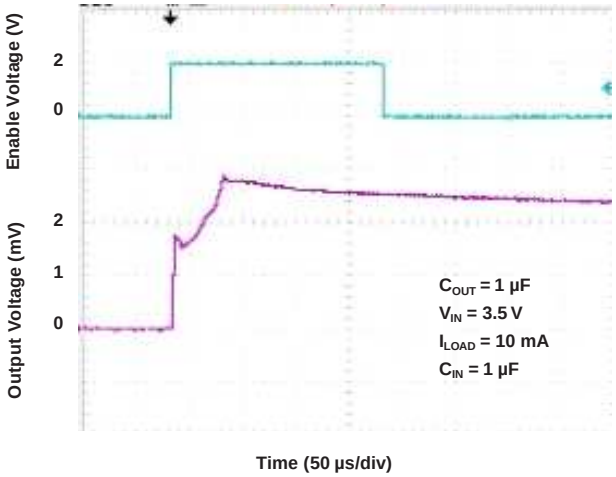


Figure 32. Turnon Time

Typical Characteristics (continued)

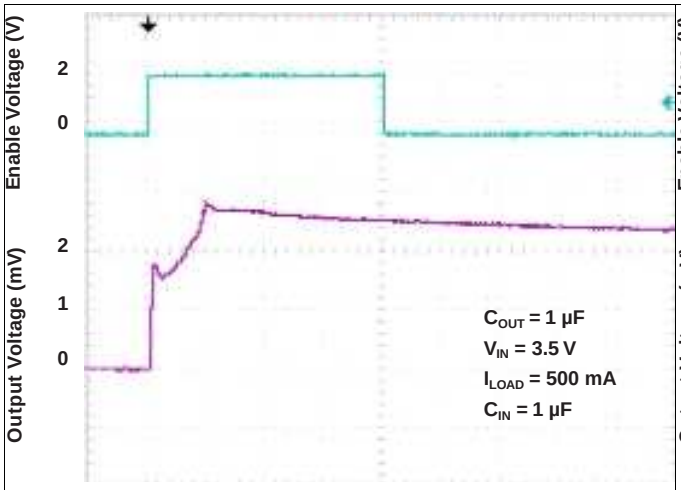


Figure 33. Turnon Time

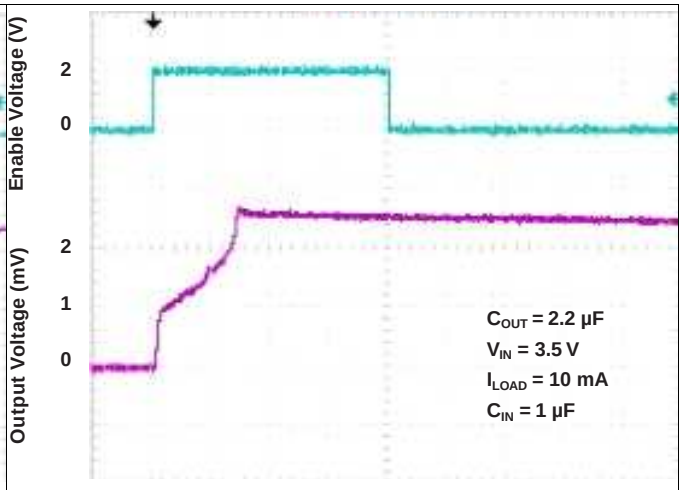


Figure 34. Turnon Time

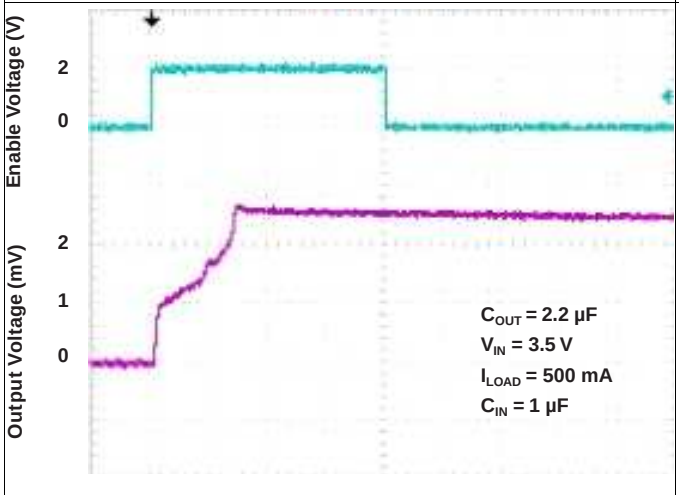


Figure 35. Turnon Time

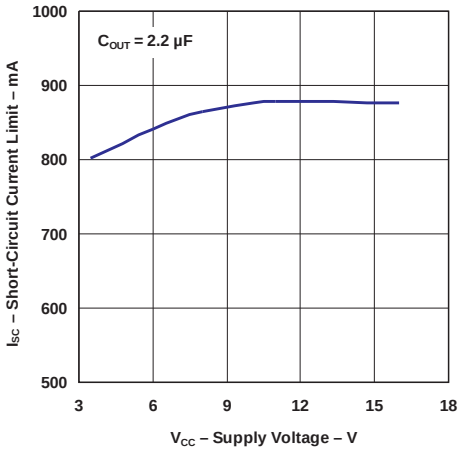


Figure 36. Short-Circuit Current vs Supply Voltage

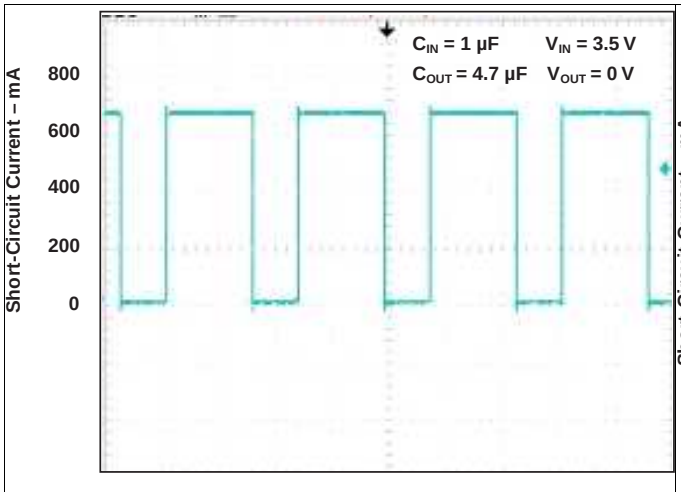


Figure 37. Short-Circuit Current vs Time

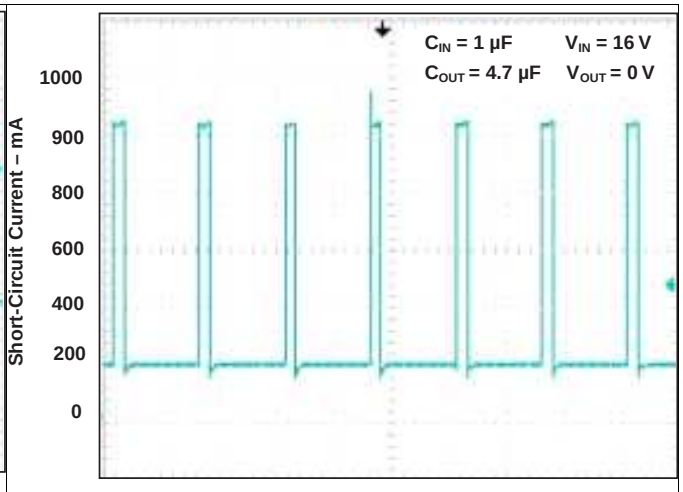


Figure 38. Short-Circuit Current vs Time

8 Detailed Description

8.1 Overview

The TL5209 device is a low-dropout (LDO) regulator with an input voltage range from 2.5 V to 16 V and a maximum output current of 500 mA. The output voltage can be adjusted using external resistors (R1 and R2) and has an accuracy of 1% to 2% depending on the ambient temperature. The maximum voltage drop across the device varies from 10 mV to 500 mV depending on the current load at the output.

8.2 Functional Block Diagram

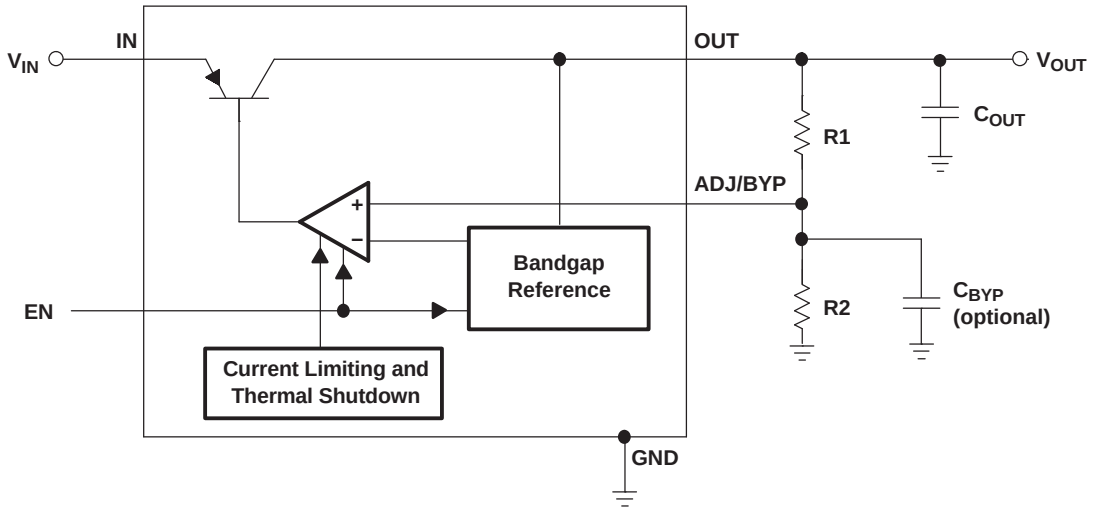


Figure 39. Low-Noise Adjustable Regulator

8.3 Feature Description

8.3.1 Enable and Shutdown

The EN pin is CMOS-logic compatible. When EN is held high (>2 V), the regulator is active. Likewise, applying a low signal (<0.4 V at 25°C) to EN or leaving it open shuts down the regulator. If the enable or shutdown feature is not needed, EN should be tied to VIN.

8.4 Device Functional Modes

The table below lists the expected value of VOUT as determined by the EN pin.

Table 1. VOUT Function Table

EN (Control Input)	VOUT
L	Open
H	1.242 V × (1 + R2/R1)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Low-Voltage Operation

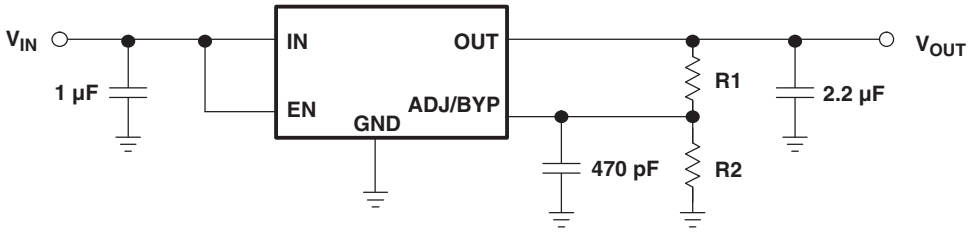
When using the TL5209 in voltage-sensitive applications, special considerations are required. If appropriate output and bypass capacitors are not chosen properly, these devices may experience a temporary overshoot of their nominal voltages.

At start-up, the full input voltage is initially applied across the regulator pass transistor, causing it to be temporarily fully turned on. By contrast, the error amplifier and voltage-reference circuits, being powered from the output, are not powered up as fast. To slow down the output ramp and give the error amplifier time to respond, select larger values of output and bypass capacitors. The longer ramp time of the output allows the regulator enough time to respond and keeps the output from overshooting its nominal value.

To prevent an overshoot when starting up into a light load (≠100 µA), TI recommends 4.7-µF and 470-pF capacitors for the output and bypass capacitors, respectively. At higher loads, 10-µF and 470-pF capacitors should be used.

If the application is not very sensitive to regulator overshoot, both the output capacitor and bypass capacitor (if applicable) can be reduced.

9.2 Typical Application



A. V_{OUT} = 1.242 V (1 + R2/R1)

B. R2 should be ≤ 470 kΩ for optimal performance.

C. Maximum V_{OUT} = 6.75 V ± 10%

Figure 40. TL5209 Typical Application

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5 V
R1	100 kΩ
Load current	500 mA
Desired V_{OUT}	3.3 V

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Output Voltage

The TL5209 develops a 1.242-V reference voltage, V_{REF}, between the output and the adjust terminal. As shown in Figure 40, this voltage is applied across resistor R1 to generate a constant current. The current I_{ADJ} from the ADJ terminal could introduce DC offset to the output. Because, this offset is very small (about 50 nA), it can be ignored. The constant current then flows through the output set resistor R2 and sets the output voltage to the desired level. Equation 1 is used for calculating VOUT:

$$VOUT = 1.242\ V \times (1 + R2 / R1) \quad (1)$$

With an R1 resistance of 100 kΩ and a desired output voltage of 3.3 V, the value for R2 can be calculated:

$$3.3\ V = 1.242\ V \times (1 + R2 / 100\ k\Omega) \quad (2)$$

$$100\ k\Omega \times ((3.3\ V / 1.242\ V) - 1) = R2 \quad (3)$$

$$R2 = 165.7\ k\Omega \quad (4)$$

Therefore, with an R2 resistance of 165.7 kΩ, the output voltage can be set to 3.3 V.

The TL5209 adjustable output should not be adjusted above 6.75 V ± 10% due to the internal Zener diode clamping the output voltage above 6.75 V. Although I_{ADJ} is very small, R2 should be limited to less than 470 kΩ for optimum performance.

9.2.2.2 Input Capacitor

If the input of the regulator is located more than ten inches from the power-supply filter, or if a battery is used to power the regulator, TI recommends a minimum 1-µF input capacitor.

9.2.2.3 Output Capacitor

As with all PNP regulators, an output capacitor is needed for stability. The required minimum size of this output capacitor depends on several factors, one of which is whether a bypass capacitor is used.

- With no bypass capacitor, TI recommends a minimum C_{OUT} of 1 µF.
- With a bypass capacitor of 470 pF (see Figure 40), TI recommends a minimum C_{OUT} of 2.2 µF.
- Larger values of C_{OUT} are beneficial, because they improve the regulator transient response.

Another factor that can determine the minimum size of the output capacitor is the load current. At low loads, a smaller output capacitor is needed for stability.

The equivalent series resistance (ESR) of the output capacitor also can affect regulator stability. C_{OUT} should have an ESR of ≠1 Ω, and it should have a resonant frequency greater than 1 MHz. Too low of an ESR can cause the output to have a low-amplitude oscillation and/or underdamped transient response. Most tantalum or aluminum electrolytic capacitors can be used for the output capacitors. However, care must be taken at low temperatures, because aluminum electrolytics use electrolytes that can freeze at low temperature (≠ –30°C). Solid tantalum capacitors do not exhibit this problem and should be used below –25°C.

9.2.2.4 Bypass Capacitor

An optional bypass capacitor, C_{BYP}, can be externally connected to the regulator through the BYP pin for improved noise performance. Connected to the internal voltage divider and the error amplifier of the regulator, this bypass capacitor filters the noise of the internal reference and reduces the noise effects on the error amplifier. The overall result is a significant drop in output noise of the regulator. TI recommends a 470-pF bypass capacitor.

Adding a bypass capacitor has several effects on the regulator that must be taken into account. First, the bypass capacitor reduces the phase margin of the regulator and, thus, the minimum C_{OUT} needs to be increased to 2.2 µF, as previously mentioned. Second, upon start-up of the regulator, the bypass capacitor has an effect on the regulator turnon time. If a slow ramp-up of the output is needed, larger values of C_{BYP} should be used. Conversely, if a fast ramp-up of the output is needed, use a smaller C_{BYP} or none at all.

If a bypass capacitor is not needed, BYP should be left open.

9.2.3 Application Curves

Figure 41 shows the expected output voltage versus R2 for various values of R1.

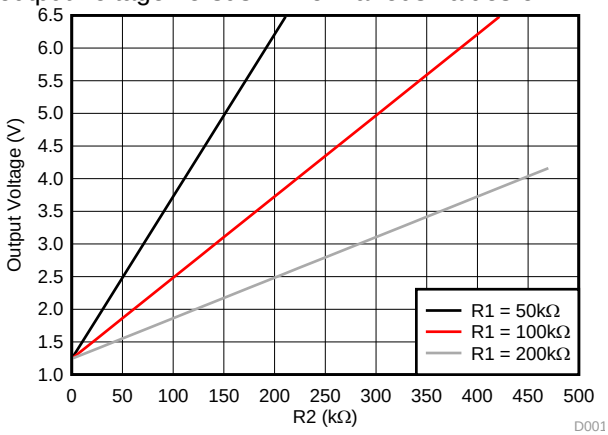


Figure 41. Expected Output Voltage vs R2 Resistance

10 Power Supply Recommendations

The device is designed to operate with an input voltage range of 2.5 V to 16 V. This supply must be well regulated and placed as close to the device terminals as possible. It must also be able to withstand all transient and load currents, using a recommended input capacitance of 1 µF if necessary. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

For best performance, VIN, VOUT, and GND traces must be as short and wide as possible to help minimize the parasitic electrical effects. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation.

11.2 Layout Example

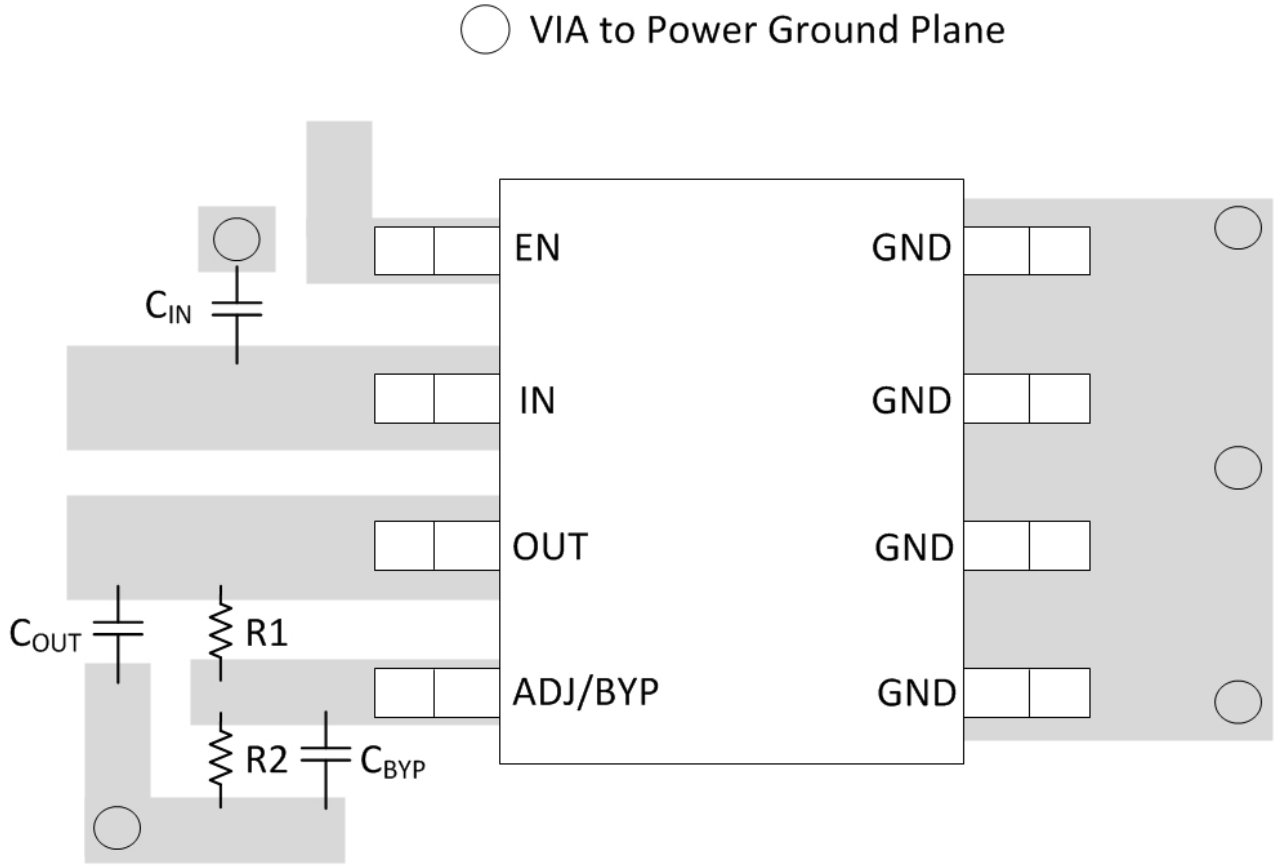


Figure 42. TL5209 Layout Schematic

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL5209DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL5209
TL5209DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL5209
TL5209DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL5209

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

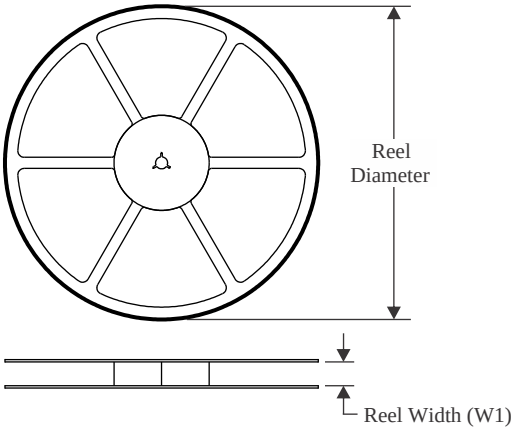
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

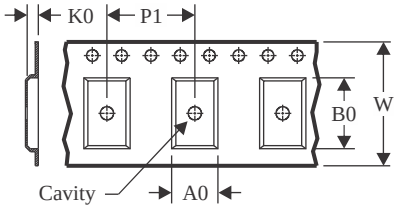
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

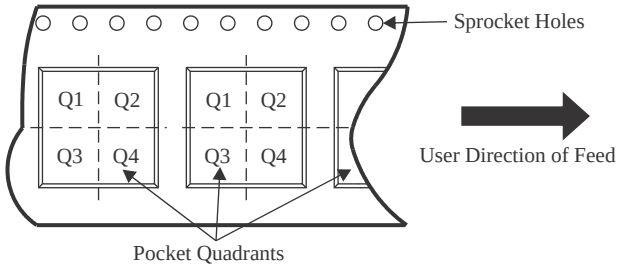


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

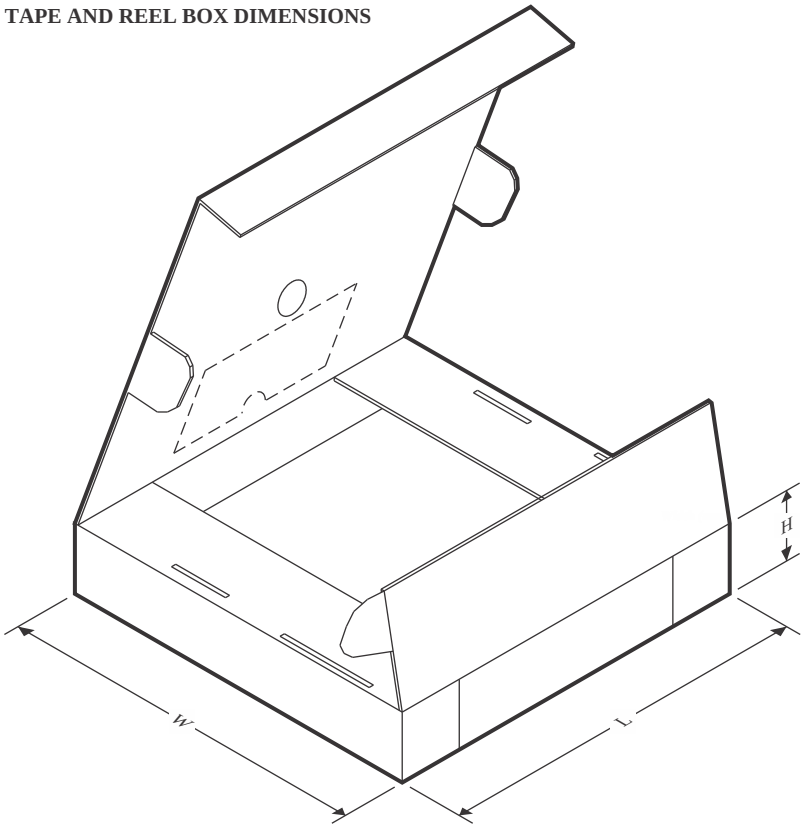
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

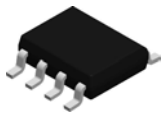
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5209DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5209DR	SOIC	D	8	2500	353.0	353.0	32.0

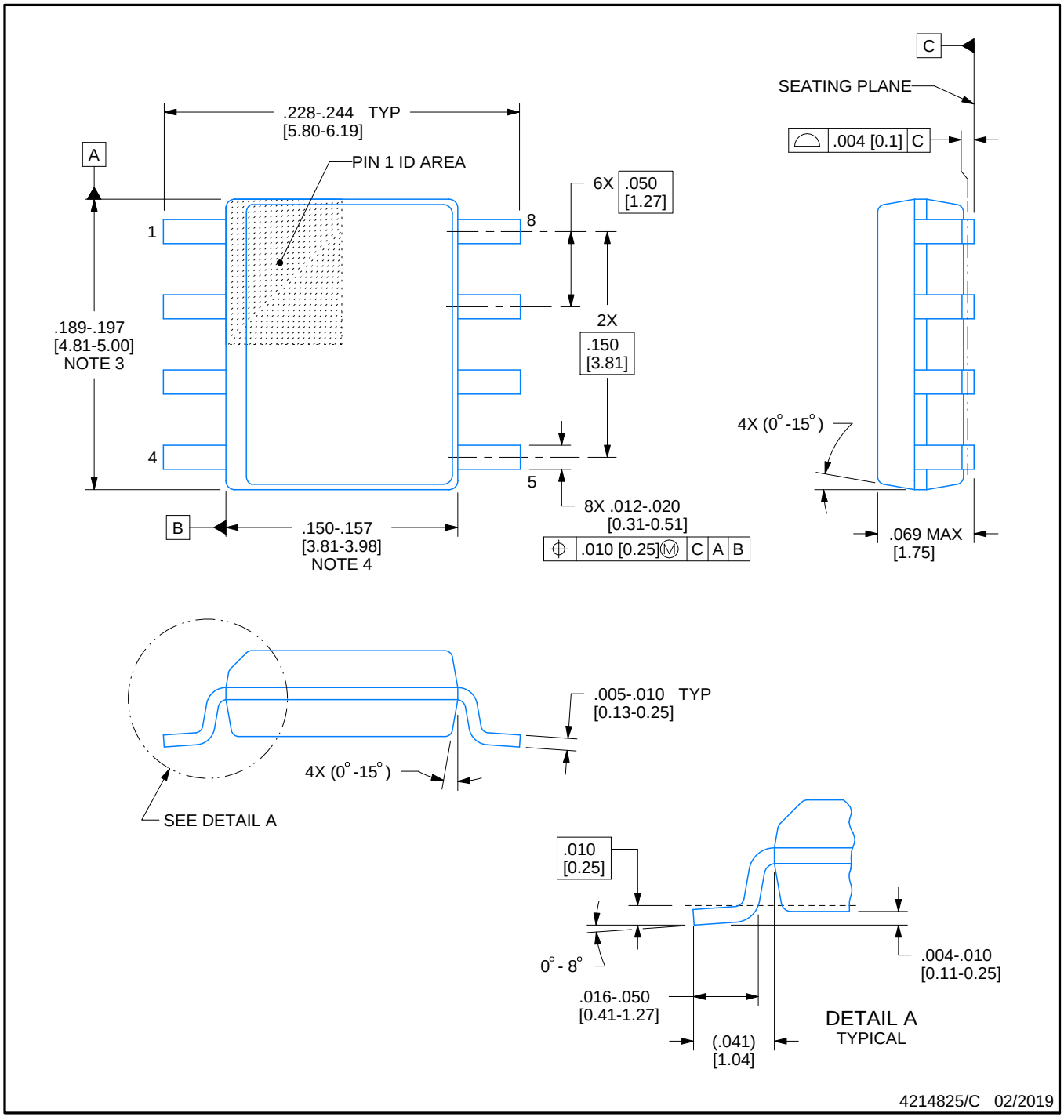


PACKAGE OUTLINE

D0008A

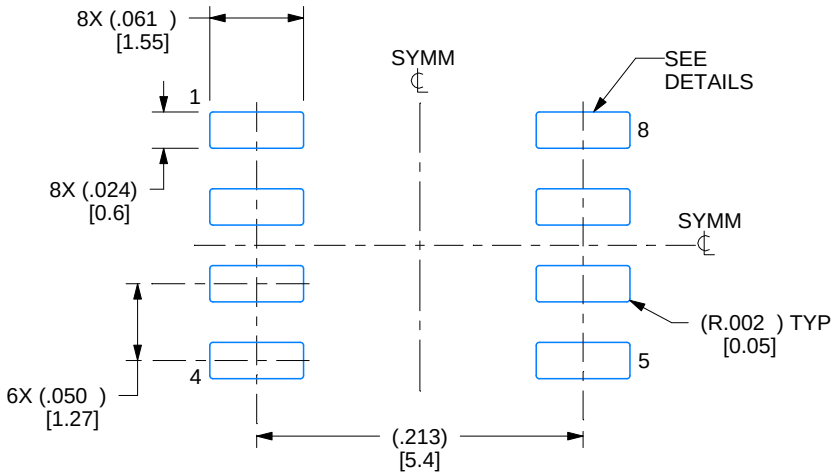
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

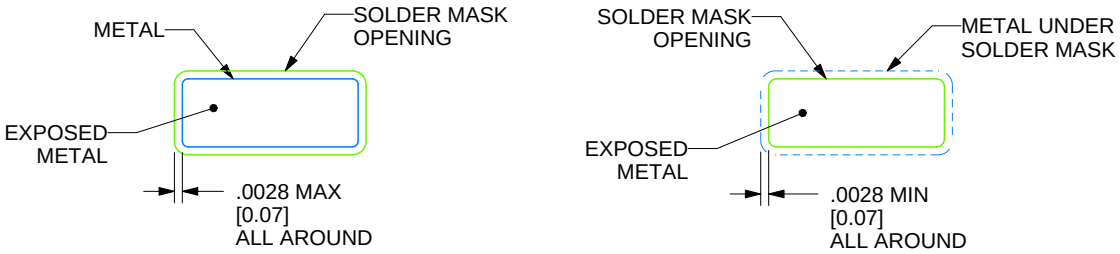


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

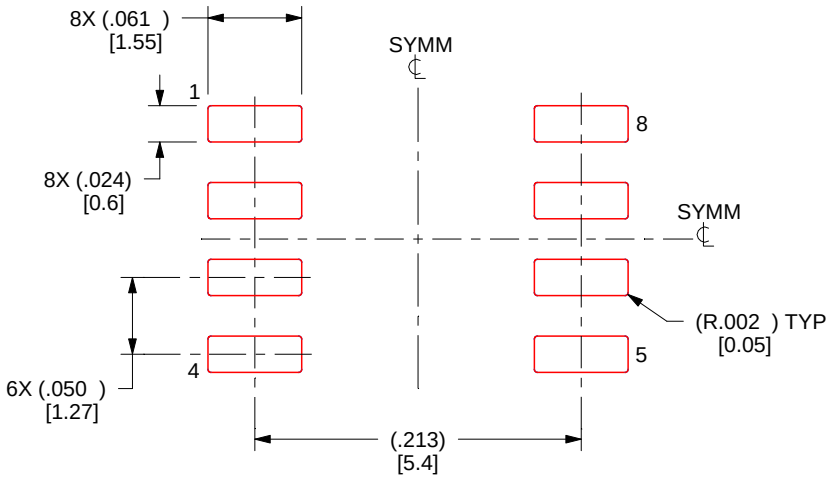
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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