TCAN114x-Q1 Enhanced CAN FD Transceiver with Partial Networking

1 Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2016
- TCAN1145-Q1 and TCAN1146-Q1 provide support for selective wake/partial networking while transmitting/receiving error-free Classic CAN or CAN FD data.
- CAN FD communication rates up to 5 Mbps
- Functional Safety Quality-Managed (TCAN1144-Q1 and TCAN1146-Q1)
  - Documentation available to aid functional safety system design
- Functional Safety-Capable (TCAN1145-Q1)
  - Documentation available to aid functional safety system design
- The TCAN114x-Q1 supports nominal processor IO voltages from 1.8 V to 5 V
- Wide operating range:
  - ±58-V Bus fault protection
  - ±12-V Common mode
- TCAN1144-Q1 and TCAN1146-Q1 support:
  - Watchdog: Timeout, Window and Q&A
  - Bus fault diagnostics and reporting
  - Programmable INH/LIMP pin
- 14-Pin SOIC, VSON and SOT23 packages
  - VSON package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Automotive infotainment and cluster
- Hybrid, electric and powertrain systems
- Industrial transportation

3 Description

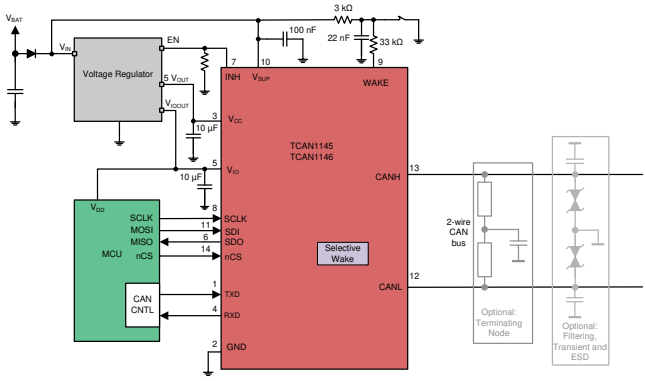
The TCAN114x-Q1 is a family of enhanced high-speed, CAN FD transceivers supporting data rates up to 5 Mbps. The devices are configured using serial peripheral interface (SPI) for access to full functionality. The TCAN114x-Q1 supports nominal processor IO voltages from 1.8 V to 5 V by applying the appropriate voltage to the V_{IO} pin, allowing lower power processors to be used.

The TCAN1145-Q1 and TCAN1146-Q1 transceivers support selective wake (being able to wake-up based on WUF identification). This feature enables systems to implement partial networking and operate with a reduced number of nodes in an active state while the remaining nodes are in a low-power sleep mode). The transceivers and selective wake function meet the specifications of the ISO 11898-2:2016 standard.

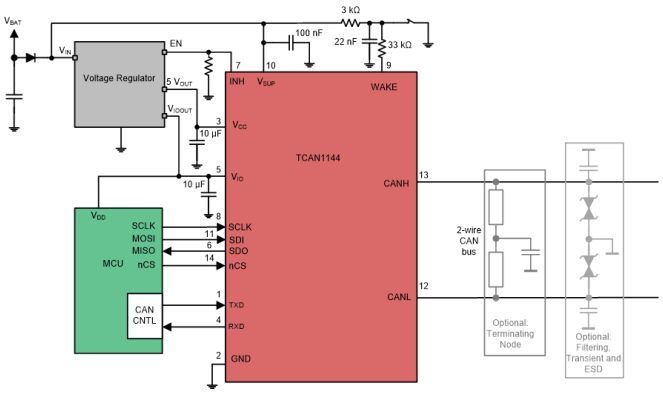
The TCAN1144-Q1 and TCAN1146-Q1 are full featured devices supporting watchdog and advanced bus diagnostics. For ease of debug, the advanced bus fault diagnostics and communication feature can be used to determine specific bus faults.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCAN114x-Q1	SOIC (D) (14)	8.65 mm x 3.9 mm
	VSON (DMT) (14)	4.5 mm x 3.0 mm
	SOT23 (DYY) (14)	4.2 mm x 2.0 mm



Simplified Schematics



Simplified Schematics

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2020) to Revision B (March 2022)	Page
• Changed *Feature*: Advanced bus fault diagnostics and reporting To: Bus fault diagnostics and reporting	1
• Changed wake up To: wake-up throughout the document	1
• Fixed the SOT23 package name from DDY to DYY	1
• Changed WAKE Absolute Minimum voltage from -0.3V to -18V in the Absolute Maximum Ratings table	5
• Changed $t_{Bit(Bus)5M}$ maximum from 210ns to 205ns in CAN FD Bit Timing	10
• Changed the WUF DLC Validation (TCAN1145-Q1 and TCAN1146-Q1) section	40

Changes from Revision * (October 2019) to Revision A (November 2020)	Page
• Multiple changes to the *Advanced Information* data sheet	1

5 Description continued

The TCAN114x-Q1 is a family of enhanced high-speed CAN FD transceivers that are register compatible enabling system designers the flexibility to implement features needed without hardware modifications and with minimal software changes. The TCAN1144-Q1 and TCAN1146-Q1 inhibit (INH) pin can be used to either enable node power or be configured as a limp home pin when a watchdog error takes place.

6 Device Comparison Table

Device Number	Selective Wake	Watchdog	Bus Fault Diagnostics	Limp Home Capable	SOIC	VSON	SOT
TCAN1144D-Q1		X	X	X	X		
TCAN1144DMT-Q1		X	X	X		X	
TCAN1144DYY-Q1		X	X	X			X
TCAN1145D-Q1	X				X		
TCAN1145DMT-Q1	X					X	
TCAN1145DYY-Q1	X						X
TCAN1146D-Q1	X	X	X	X	X		
TCAN1146DMT-Q1	X	X	X	X		X	
TCAN1146DYY-Q1	X	X	X	X			X

7 Pin Configuration and Functions

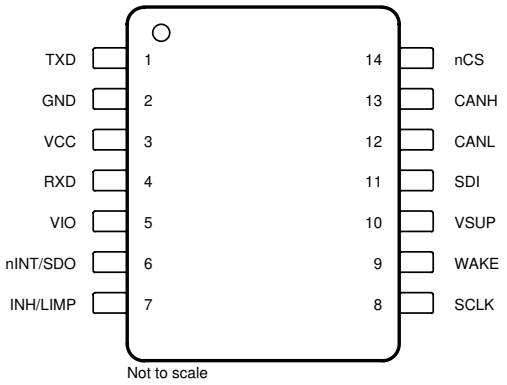


Figure 7-1. D Package, 14 Pin (SOIC), Top View

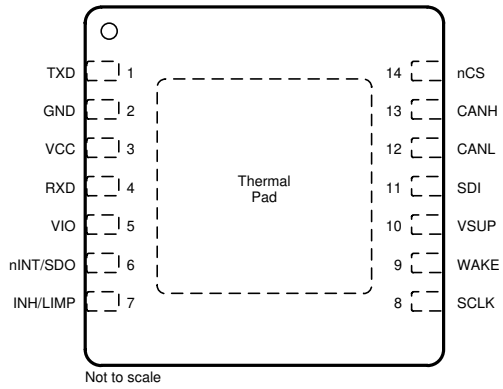


Figure 7-2. DMT Package, 14 Pin (VSON), Top View

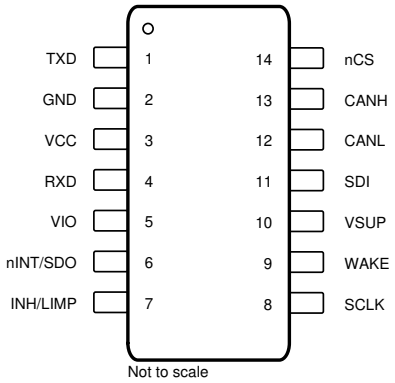


Figure 7-3. DYY Package, 14 Pin (SOT-23), Top View

Table 7-1. Pin Functions

PIN		TYPE[2]	DESCRIPTION
NO.	NAME		
1	TXD	DI	CAN transmit data input (low for dominant and high for recessive bus states)
2	GND	GND	Ground connection[1]
3	V_{CC}	P	5 V CAN bus supply voltage
4	RXD	DO	CAN receive data output (low for dominant and high for recessive bus states), tri-state
5	VIO	P	Digital I/O voltage supply
6	nINT/SDO	DO	Serial data output when nCS is low and nINT when nCS is high
7	INH/LIMP	HVO	Defaults to Inhibit pin to control system voltage regulators and supplies. TCAN1144-Q1 and TCAN1146-Q1 can configure this pin for a LIMP home function
8	SCLK	DI	SPI clock input
9	WAKE	HVI	Local wake input terminal
10	VSUP	HVP	High-voltage supply from the battery
11	SDI	DI	Serial data input
12	CANL	BI/O	Low level CAN bus I/O line
13	CANH	BI/O	High level CAN bus I/O line
14	nCS	DI	Chip select (active low)

(1) PAD and GND Pins must be soldered to GND
(2) DI = digital input, DO = digital output, HVI = high voltage input, HVO = high voltage output, HVP = high voltage power, P = power, BI/O = bus input/output

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range for – 40 °C ≤ TA ≤ 125 °C (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage	–0.3	42	V
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN bus I/O voltage (CANH, CANL)	–58	58	V
V_{WAKE}	WAKE input voltage	–18	42	V
V_{INH}	INH pin voltage	–0.3	42 and VO ≤ VSUP+0.3	V
V_{LOGIC}	Logic pin voltage (RXD, TXD, SPI)	–0.3	6	V
V_{SO}	Digital output terminal voltage	–0.5	6	V
$I_{O(LOGIC)}$	Logic pin output current		4	mA
$I_{O(INH/LIMP)}$	Inhibit/limp pin output current		6	mA
$I_{O(WAKE)}$	WAKE pin output current		3	mA
T_J	Junction temperature	–40	165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) Classification Level H2, V_{SUP}, CANL/H, and WAKE, per AEC Q100-002(1)		±8000	V
		Human body model (HBM) Classification Level 3A, all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) Classification Level C5, per AEC Q100-011	Corner pins (1, 7, 8, and 14)	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge per IEC 62228-3(1)	Contact discharge	±8000	V
		Indirect ESD discharge	±15000	V
$V_{(ESD)}$	Electrostatic discharge per SAE J2962-2(2)	Contact discharge	±8000	V
		Air-gap discharge	±15000	
ISO 7637-2 and IEC 62215-3 Transients per IEC 62228-3, CANH/L, V_{SUP} and WAKE(3)		Pulse 1	-100	V
		Pulse 2	75	
		Pulse 3a	-150	
		Pulse 3b	100	
ISO 7637-3 Slow Transient Pulse CAN bus terminals to GND per SAE J2962-2(4)		Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	±30	V

(1) Testing performed at 3rd party. Different system-level configurations may lead to results. Test report available upon request.
(2) SAE J2962-2 Testing performed at 3rd party approved EMC test facility, test report available upon request.
(3) ISO 7637-2 is a system-level transient test. Results given are provide by a 3rd party test house. Different system-level configurations may lead to different results. Test report available upon request.

(4) ISO 7637-3 is a system-level transient test. Results given are provide by a 3rd party test house. Different system-level configurations may lead to different results. Test report available upon request.

8.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4.5		28	V
V_{IO}	I/O supply voltage	1.71		5.5	V
V_{CC}	CAN transceiver supply voltage	4.5		5.5	V
$I_{OH(DO)}$	Digital output high level current	–2			mA
$I_{OL(DO)}$	Digital output low level current			2	mA
$I_{O(INH/LIMP)}$	Inhibit/LIMP pin current			1	mA
T_J	Junction temperature	–40		150	°C
TSDR	Thermal shut down	175			°C
TSDF	Thermal shut down release	160			°C
TSDW	Thermal shut down warning	150			°C
TSDHYS	Thermal shut down hysteresis		10		°C

8.5 Thermal Information

THERMAL METRIC(1)		TCAN114x			UNIT
		D (SOIC)	DMT (VSON)	DYY(SOT-23)	
		14-PINS	14-PINS	14-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.6	34.8	81.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.6	37.3	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.5	12.5	20.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.2	0.6	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.1	12.5	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.3	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.6 Supply Characteristics

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY FROM BATTERY						
I_{SUP}	Battery supply current	Sleep mode: selective wake off, 4.5 V ≤ V_{SUP} ≤ 28 V		20	35	µA
		Standby mode: selective wake off, 4.5 V ≤ V_{SUP} ≤ 28 V		60	95	µA
		Additional current when CAN bus is listening and bias is connected to 2.5 V.		15	40	µA
		Additional current from WAKE pin		1	2	µA
		Normal mode		1	1.5	mA
		Additional current when selective wake is enabled and bus active		400	550	µA
$V_{SUP(PU)R}$	Supply on detection	V_{SUP} rising	2.0		3.9	V
$V_{SUP(PU)F}$	Supply off detection	V_{SUP} falling	1.85		3.5	V
UV_{SUPR}	Supply under voltage recovery	V_{SUP} rising	3.75		4.4	V
UV_{SUPF}	Supply under voltage detection	V_{SUP} falling	3.4		4.25	V
SUPPLY FROM V_{CC}						

8.6 Supply Characteristics (continued)

parameters valid across -40 °C ≤ T_J ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	Normal mode: Recessive, V_{TXD} = V_{IO}		3	5	mA
		Normal mode: Dominant, V_{TXD} = 0 V, R_L = 60 Ω and C_L = open, typical bus load			60	mA
		Normal mode: Dominant, V_{TXD} = 0 V, R_L = 50 Ω and C_L = open, high bus load			70	mA
		Normal mode: Dominant with bus fault, V_{TXD} = 0 V, CANH = - 25 V, R_L and C_L = open			120	mA
		Standby mode: selective wake off, V_{TXD} = V_{CC}, R_L = 50 Ω, C_L = open		3.5	8	µA
		Sleep mode		2.5	5	µA
UV_{CCR}	Supply under voltage recovery	V_{CC} rising		4.2	4.5	V
UV_{CCF}	Supply under voltage detection	V_{CC} falling	3.5	4		V
I_{IO}	I/O supply current from V_{IO}	Sleep mode: V_{TXD} = V_{IO} where 1.71 V < VIO < 5.5 V			10	µA
I_{IO}	I/O supply current from V_{IO}	Standby mode: V_{TXD} = V_{IO}			10	µA
		Normal mode: recessive			10	µA
		Normal mode: dominant			40	µA
UV_{IOR}	Supply under voltage recovery	V_{IO} rising		1.4	1.65	V
UV_{IOF}	Supply under voltage detection	V_{IO} falling	1	1.25		V

8.7 Electrical Characteristics

parameters valid across -40 °C ≤ T_J ≤ 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN DRIVER ELECTRICAL CHARACTERISTICS						
$V_{O(D)}$	Bus output voltage (dominant) CANH	See Figure 9-4 V_{TXD} = 0 V, R_L =50 Ω to 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
	Bus output voltage (dominant) CANL		0.5		2.25	V
$V_{O(R)}$	Bus output voltage (recessive)	See Figure 9-1 and Figure 9-4 V_{TXD} = V_{IO}, R_L = open (no load), R_{CM} = open	2	2.5	3	V
$V_{(DIFF)}$	Differential voltage		–42		42	V
$V_{OD(D)}$	Differential output voltage (dominant)	See Figure 9-1 and Figure 9-4, V_{TXD} = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	V
		See Figure 9-1 and Figure 9-4, V_{TXD} = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, R_{CM} = open	1.4		3	V
		See Figure 9-1 and Figure 9-4, V_{TXD} = 0 V, R_L = 2.24 kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{OD(R)}$	Differential output voltage (recessive)	See Figure 9-1 and Figure 9-4 , V_{TXD} = V_{IO}, R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
		See Figure 9-1 and Figure 9-4, V_{TXD} = V_{IO}, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	mV
$V_{O(INACT)}$	Bus output voltage on CANH with bus biasing inactive (STBY)	See Figure 9-1 and Figure 9-4, V_{TXD} = V_{IO}, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
	Bus output voltage on CANL with bus biasing inactive (STBY)		–0.1		0.1	V
	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive (STBY)		–0.2		0.2	V
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}	See Figure 9-1 and Figure 9-4, R_L = 60 Ω, C_L = open, R_{CM} = open, C_1 = 4.7 nF, TXD = 250 kHz, 1 MHz, 2.5 MHz	0.9		1.1	V/V
V_{SYM_DC}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$) – $V_{O(CANL)}$)) with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, <1 MHz or <2 Mbit/s	See Figure 9-1 and Figure 9-4, R_L = 60 Ω, C_L = open, R_{CM} = open, C_1 = 4.7 nF	–300		300	mV

8.7 Electrical Characteristics (continued)

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS_DOM}	Short-circuit steady-state output current, dominant See Figure 9-1 and Figure 9-8	–3.0 V ≤ V_{CANH} ≤ +18.0 V, CANL = open, V_{TXD} = 0 V	–115			mA
		–3.0 V ≤ V_{CANL} ≤ +18.0 V, CANH = open, V_{TXD} = 0 V			115	mA
I_{OS_REC}	Short-circuit steady-state output current, recessive. See Figure 9-1 and Figure 9-8	–27 V ≤ V_{BUS} ≤ +42 V, V_{BUS} = CANH = CANL	–5		5	mA
CAN RECEIVER ELECTRICAL CHARACTERISTICS						
V_{ITDOM}	Receiver dominant state differential input voltage range, bus biasing active	–12.0 V ≤ V_{CANL} ≤ +12.0 V –12.0 V ≤ V_{CANH} ≤ +12.0 V; See Figure 9-5 and Table 10-6	0.9		8	V
V_{ITREC}	Receiver recessive state differential input voltage range, bus biasing active		–3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal and selective wake modes			135		mV
V_{DIFF_DOM}	Receiver dominant state differential input voltage range, bus biasing in-active	–12.0 V ≤ V_{CANL} ≤ +12.0 V –12.0 V ≤ V_{CANH} ≤ +12.0 V; See Figure 9-5 and Table 10-6	1.15		8	V
V_{DIFF_REC}	Receiver recessive state differential input voltage range, bus biasing in-active		–3		0.4	V
V_{CM_NORM}	Common mode range: normal		–12		12	V
V_{CM_STBY}	Common mode range: standby mode		–12		12	V
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = V_{sup} to GND via 0 Ω and 47 kΩ resistor			5	µA
C_I	Input capacitance to ground (CANH or CANL) (1)				20	pF
C_{ID}	Differential input capacitance (1)				10	pF
R_{ID}	Differential input resistance	V_{TXD} = V_{IO}, normal mode: –2.0 V ≤ V_{CANH} ≤ +7.0 V; –2.0 V ≤ V_{CANL} ≤ +7.0 V	12		100	kΩ
R_{IN}	Single ended Input resistance (CANH or CANL)	–2.0 V ≤ V_{CANH} ≤ +7.0 V –2.0 V ≤ V_{CANL} ≤ +7.0 V	6		50	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5.0 V	–1		1	%
INH OUTPUT TERMINAL (HIGH VOLTAGE OUTPUT)						
ΔV_H	High-level voltage drop from V_{SUP} to INH	I_{INH} = –6 mA		0.5	1	V
R_{pd}	Pull-down resistor	Sleep Mode	7	10	13	MΩ
WAKE INPUT TERMINAL						
V_{IH}	High-level input voltage	Selective wake-up or standby mode, WAKE pin enabled	4			V
V_{IL}	Low-level input voltage	Selective wake-up or standby mode, WAKE pin enabled			2	V
I_{IL}	Low-level input current	WAKE = 1 V		1	2	µA
SDI, SCK, nCS, TXD INPUT TERMINALS						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	1.71 V ≤ V_{IO} ≤ 5.5 V	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, 1.71 V ≤ V_{IO} ≤ 5.5 V	–30		–2	µA
I_{ILnCS}	Low-level input leakage current for nCS	Inputs = 0 V, 1.71 V ≤ V_{IO} ≤ 5.5 V	–50		–2	µA
C_{IN}	Input capacitance	at 20 MHz	4		15	pF
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5 V, V_{IO} = V_{SUP} = 0 V	–1	0	1	µA
Rpu	Pull-up resistor		250	350	450	kΩ
RXD, SDO OUTPUT TERMINALS						
V_{OH}	High level output voltage	I_{OH} = -2 mA	0.8			V_{IO}
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current - SDO pin	V_{nCS} = V_{IO}; V_O = 0 V to V_{IO}	–5		5	µA

8.7 Electrical Characteristics (continued)

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{RXD(PU)}$	RXD pin pull-up resistance	Active during UV_{SUP} and POR conditions and when in Sleep mode	40	60	80	kΩ
$I_{LKG(RXD)}$	RXD current when V_{IO} present and $R_{RXD(PU)}$ enabled	V_{RXD} = V_{IO}; V_O = 0 V to V_{IO}	–1		1	µA
		V_{RXD} = GND; Active during UV_{SUP} and POR conditions and when in Sleep mode	–140		–20	µA

(1) Specified by design

8.8 Timing Requirements

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY					
t_{PWRUP}	Time from V_{SUP} exceeding4.4 V until INH active; see Figure 9-12		2	4	ms
t_{UVFLTR}	Under voltage detection delay time	3		50	µs
t_{UVSLP}	Time from an UV_{CC} and/or UV_{IO} event to clear before transitioning to sleep or failsafe mode	200		400	ms
MODE CHANGE					
$t_{MODE\_STBY\_NOM}$	The time it takes for the part to transition to normal mode from standby mode after receiving this command via SPI			70	µs
$t_{MODE\_NOM\_SLP}$	The time it takes for the part to transition to sleep mode from normal mode after receiving this command via SPI; see Figure 9-14			200	µs
$t_{MODE\_SLP\_STBY}$	Time from UV_{CC} and UV_{IO} clearing after INH turns on to RXD pin pulling low; (3) see Figure 9-13			100	µs
$t_{MODE\_NOM\_STBY}$	The time it takes for the part to transition to standby mode from normal mode after receiving this command via SPI; see Figure 9-15			70	µs
$t_{INH\_SLP\_STBY}$	WUP, LWU or WUF event until INH asserted; see Figure 9-13			100	µs
$t_{INH\_NOM\_SLP}$	SPI write to go to sleep from normal mode and INH turns off; see Figure 9-14			50	µs
DEVICE TIMING					
t_{WAKE}	Wake up time from a wake edge on WAKE; standby, selective wake or sleep mode; See Figure 10-14 and Figure 10-15	40			µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out; See Figure 10-14 and Figure 10-15			10	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value; see Figure 10-12	0.5		2	ms
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake-up request; see Figure 10-12	0.5		1.8	µs
$t_{WK\_WIDTH\_MIN}$ (4)	Minimum WAKE Pin pulse width (1) (2) Register 11h[3:2] = 00b; see Figure 10-16	10			ms
	Minimum WAKE Pin pulse width (1) (2) Register 11h[3:2] = 01b; see Figure 10-16	20			ms
	Minimum WAKE Pin pulse width (1) (2) Register 11h[3:2] = 10b; see Figure 10-16	40			ms
	Minimum WAKE Pin pulse width (1) (2) Register 11h[3:2] = 11b; see Figure 10-16	80			ms
$t_{WK\_WIDTH\_INVALID}$	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 00b; see Figure 10-16			5	ms
	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 01b; see Figure 10-16			10	ms
	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 10b; see Figure 10-16			20	ms
	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 11b; see Figure 10-16			40	ms

8.8 Timing Requirements (continued)

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{WK\_WIDTH\_MAX}$	Maximum WAKE Pin pulse window (1) Register 11h[1:0] = 00b; see Figure 10-16	750		950	ms
	Maximum WAKE Pin pulse window (1) Register 11h[1:0] = 01b; see Figure 10-16	1000		1250	ms
	Maximum WAKE Pin pulse window (1) Register 11h[1:0] = 10b; see Figure 10-16	1500		1875	ms
	Maximum WAKE Pin pulse window (1) Register 11h[1:0] = 11b; see Figure 10-16	2000		2500	ms
$t_{SILENCE}$	Timeout for bus inactivity. Timer is reset and restarted when bus changes from dominant to recessive or vice versa.	0.6		1.2	s
$t_{INACTIVE}$	SWE timer used for failsafe and power up inactivity	3.75		5	min
t_{Bias}	Time from the start of a dominant-recessive-dominant sequence. Each phase 6 µs until Vsym ≥ 0.1; see Figure 9-9			250	µs
t_{TXD_DTO}	Dominant time out, R_L = 60 Ω, C_L = open; see Figure 9-7	1		5	ms
t_{TOGGLE}	RXD pin toggle timing when programmed after a WUP; see Figure 10-12	5	10	15	µs

(1) This parameter is valid only when register 11h[7:6] = 11b
(2) This is the minimum pulse width for a WAKE pin input that device will detect as a good pulse. Values between the min $t_{WK\_WIDTH\_MIN}$ and max $t_{WK\_WIDTH\_INVALID}$ are indeterminate and may or may not be considered valid. This parameter works with $t_{WK\_WIDTH\_MIN}$ to determine if a WAKE input pulse is valid
(3) Dependent upon V_{CC} and V_{IO} being above UV_{CC} and UV_{IO} after INH turns on node power.
(4) $t_{WK\_WIDTH\_INVALID}$ sets this value by using register 11h[3:2]

8.9 Switching Characteristics

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN TRANSCEIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, high TXD to driver recessive	Typical conditions: R_L = 60 Ω, C_L = 100 pF, R_{CM} = open; see Figure 9-4	50	85	110	ns
t_{pLD}	Propagation delay time, low TXD to driver dominant		35	85	110	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			30	40	ns
$t_{R/F}$	Differential output signal rise time		5	55	75	ns
t_{pRH}	Propagation delay time, bus recessive input to high RXD output	Typical conditions: CANL = 1.5 V, CANH = 3.5 V; see Figure 9-5	25	75	150	ns
t_{pDL}	Propagation delay time, bus dominant input to low RXD output		25	75	110	ns
t_{LOOP}	Loop Delay(1)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, 3.0 V ≤ V_{IO} ≤ 5.5 V			215	ns
		Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, 1.72 V ≤ V_{IO} < 3.0 V			225	ns
CAN FD BIT TIMING						
$t_{Bit(Bus)2M}$	Transmitted recessive bit width @ 2 Mbps	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF; see Figure 9-6	440		525	ns
$t_{Bit(Bus)5M}$	Transmitted recessive bit width @ 5 Mbps		160		205	ns
$t_{Bit(RXD)2M}$	Received recessive bit width @ 2 Mbps	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF; see Figure 9-6	410		540	ns
$t_{Bit(RXD)5M}$	Received recessive bit width @ 5 Mbps		130		210	ns
Δt_{Rec}	Receiver Timing symmetry @ 2 Mbps, intended for use with bit rates above 1 Mbps up to 2 Mbps	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	–60	5	35	ns
	Receiver Timing symmetry @ 5 Mbps, intended for use with bit rates above 2 Mbps up to 5 Mbps		–45		10	ns
SPI SWITCHING CHARACTERISTICS						
f_{SCK}	SCK, SPI clock frequency	Normal, standby, listen and failsafe modes			4	MHz
		Sleep mode: If V_{IO} is present			10	kHz

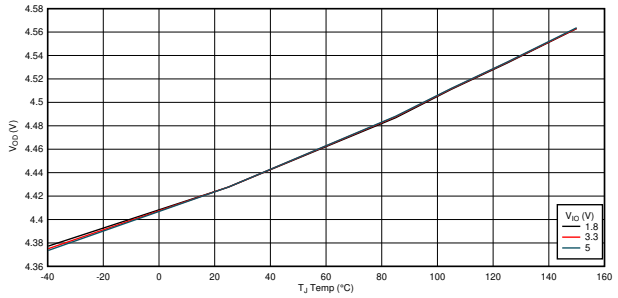
8.9 Switching Characteristics (continued)

parameters valid across -40 ℃ ≤ T_J ≤ 150 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SCK}	SCK, SPI clock period	Normal, standby, listen and failsafe modes; see Figure 9-11	250			ns
		Sleep mode: If If V_{IO} is present; See Figure 9-11	100			µs
t_{RSCK}	SCK rise time	See Figure 9-10			40	ns
t_{FSCK}	SCK fall time	See Figure 9-10			40	ns
t_{SCKH}	SCK, SPI clock high	Normal, standby, listen and failsafe modes; see Figure 9-11	125			ns
		Sleep mode: If V_{IO} is present; See Figure 9-11	500			ns
t_{SCKL}	SCK, SPI clock low	Normal, standby, listen and failsafe modes; see Figure 9-11	125			ns
		Sleep mode: If V_{IO} is present	500			ns
t_{CSS}	Chip select setup time	See Figure 9-10	100			ns
t_{CSH}	Chip select hold time	See Figure 9-10	100			ns
t_{CSD}	Chip select disable time	See Figure 9-10	50			ns
t_{SISU}	Data in setup time	Normal, standby, listen and failsafe modes; see Figure 9-10	50			ns
		Sleep mode: If V_{IO} is present; see Figure 9-10	200			ns
t_{SIH}	Data in hold time	Normal, standby, listen and failsafe modes; see Figure 9-10	50			ns
		Sleep mode: If V_{IO} is present; see Figure 9-10	200			ns
t_{SOV}	Data out valid	Normal, standby, listen and failsafe modes; see Figure 9-11			80	ns
		Sleep mode: If V_{IO} is present; see Figure 9-11			200	ns
t_{RSO}	Data out rise time	See Figure 9-11			40	ns
t_{FSO}	Data out fall time	See Figure 9-11			40	ns

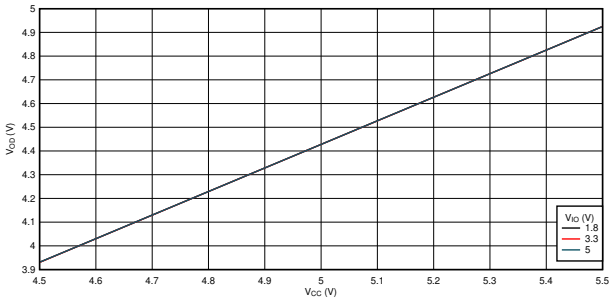
(1) Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.

8.10 Typical Characteristics



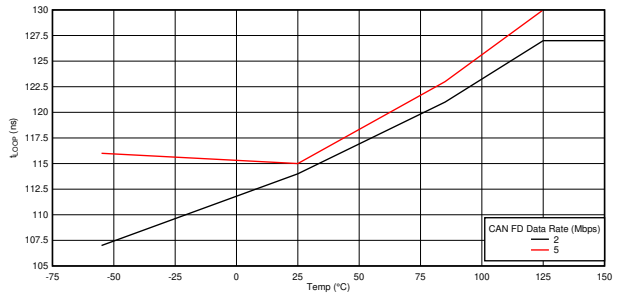
V_{SUP} = 12 V V_{CC} = 5 V

Figure 8-1. VOD vs Temperature



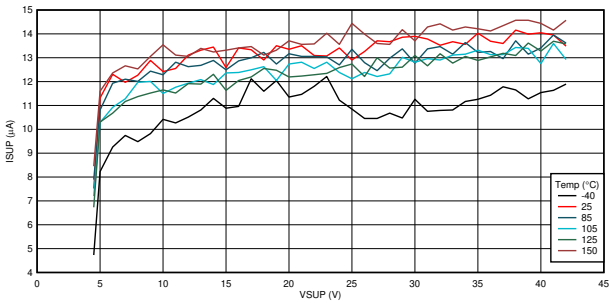
V_{SUP} = 12 V Temperature = 25 ºC

Figure 8-2. VOD vs VCC



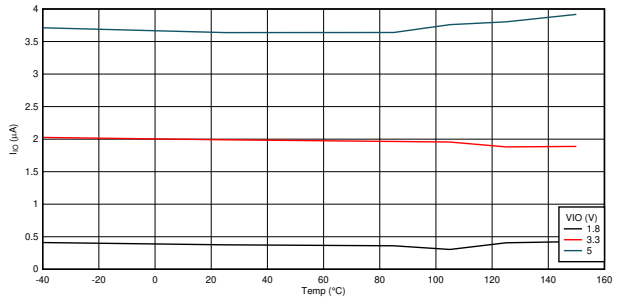
V_{SUP} = 12 V V_{CC} = 5 V V_{IO} = 3.3 V

Figure 8-3. t_{LOOP} vs Temperature



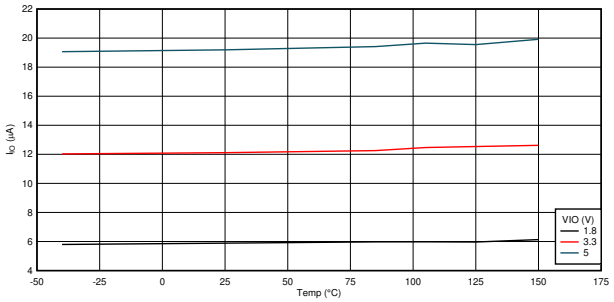
V_{CC} = 5 V V_{IO} = 3.3 V

Figure 8-4. Sleep Mode: ISUP vs Temperature



V_{SUP} = 12 V V_{CC} = 5 V

Figure 8-5. Normal Mode: I_{IO} vs Temperature Recessive



V_{SUP} = 12 V V_{CC} = 5 V

Figure 8-6. Normal Mode: I_{IO} vs Temperature Dominant

9 Parameter Measurement Information

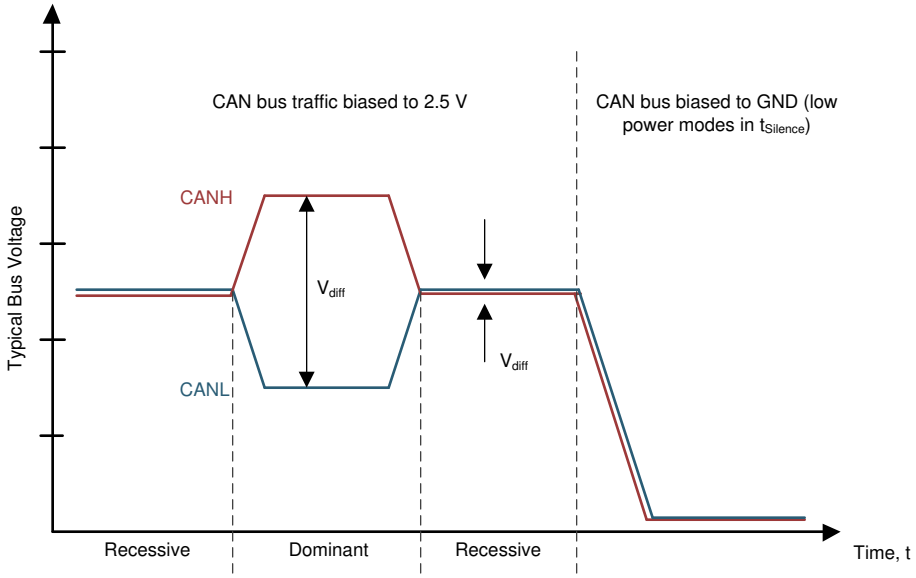


Figure 9-1. Bus States (Physical Bit Representation)

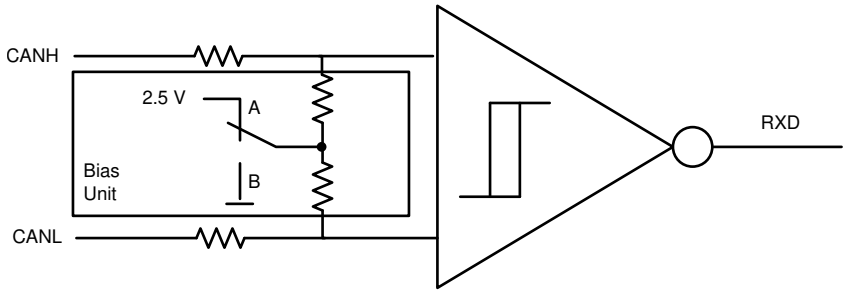


Figure 9-2. Simplified Recessive Common Mode Bias Unit and Receiver

Note

A: Normal and Listen modes or all other modes not in $t_{Silence}$

- Selective wake supported by TCAN1145-Q1 and TCAN1146-Q1

B: All modes except Normal and Listen modes, in $t_{Silence}$

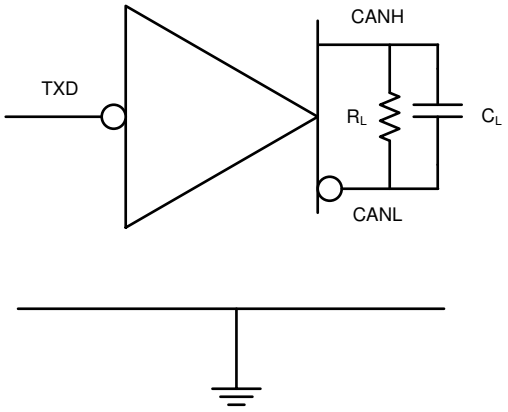


Figure 9-3. Supply Test Circuit

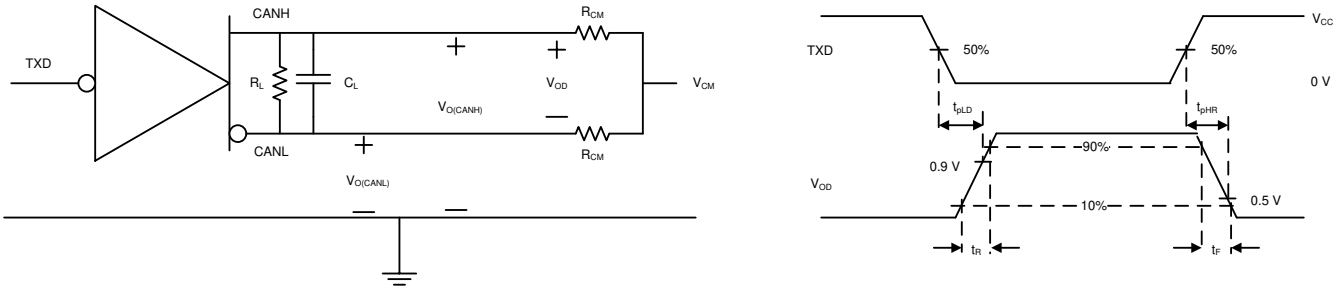


Figure 9-4. Driver Test Circuit and Measurement

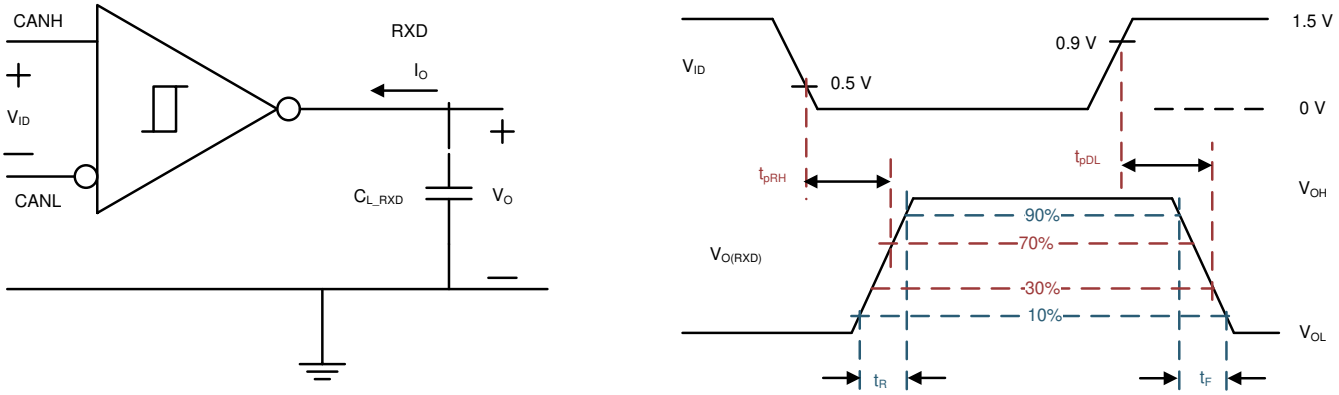


Figure 9-5. Receiver Test Circuit and Measurement

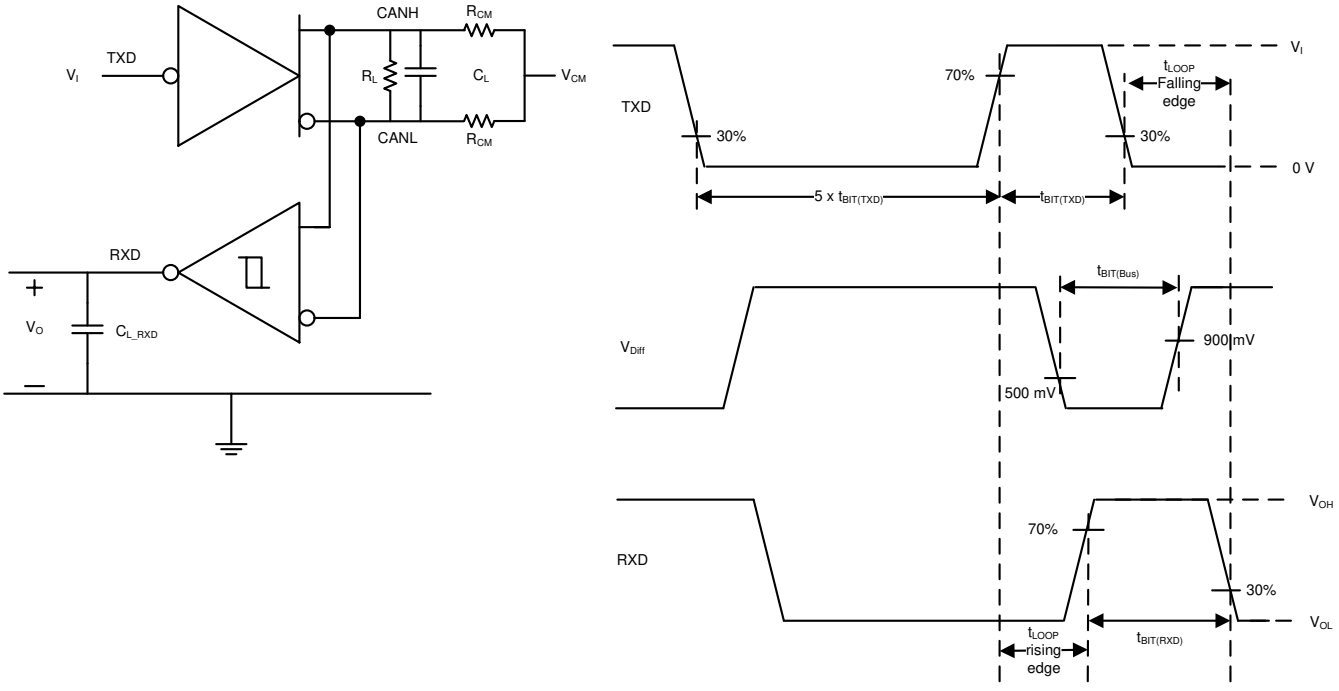


Figure 9-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

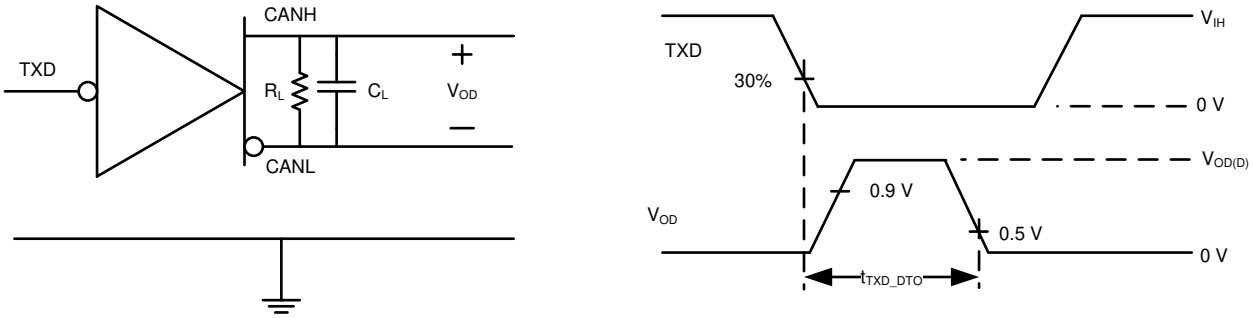


Figure 9-7. TXD Dominant Time Out Test Circuit and Measurement

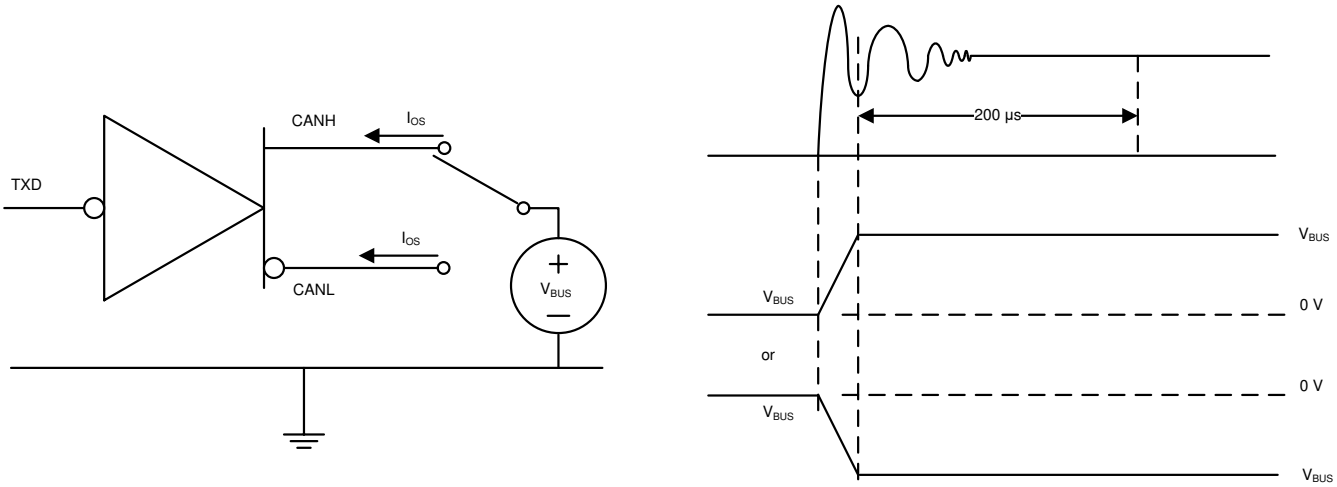


Figure 9-8. Driver Short-Circuit Current Test and Measurement

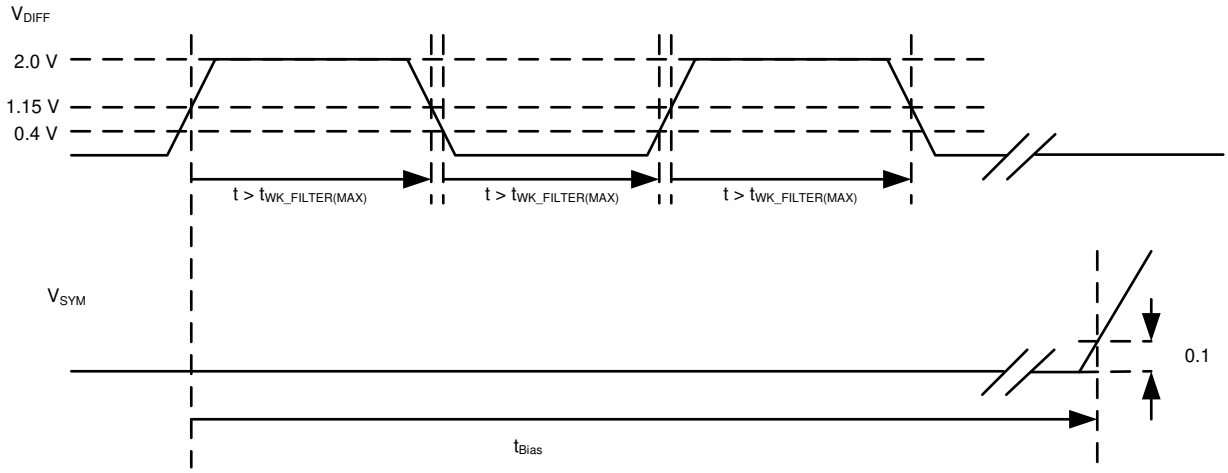


Figure 9-9. Test Signal Definition for Bias Reaction Time Measurement

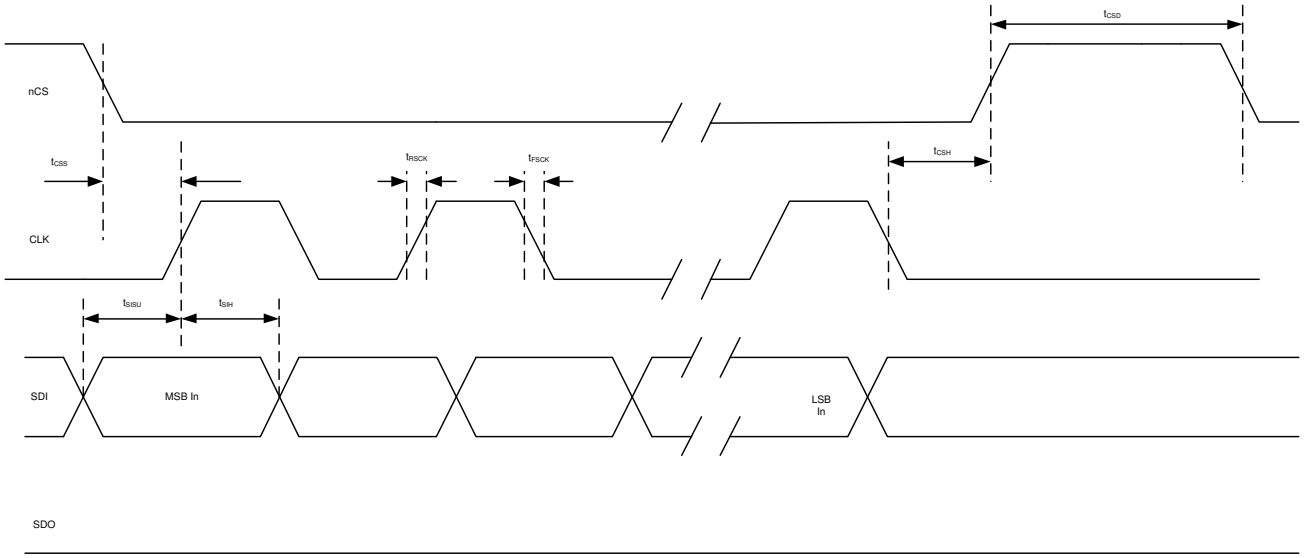


Figure 9-10. SPI AC Characteristic Write

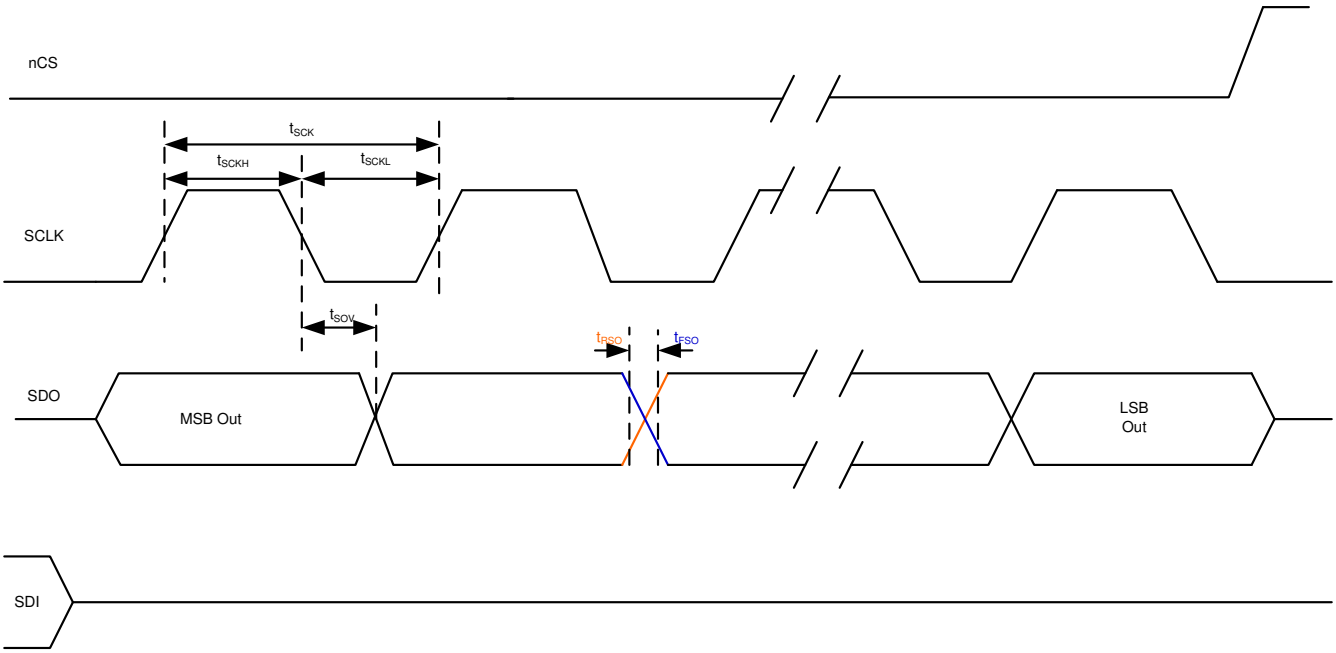


Figure 9-11. SPI AC Characteristic Read

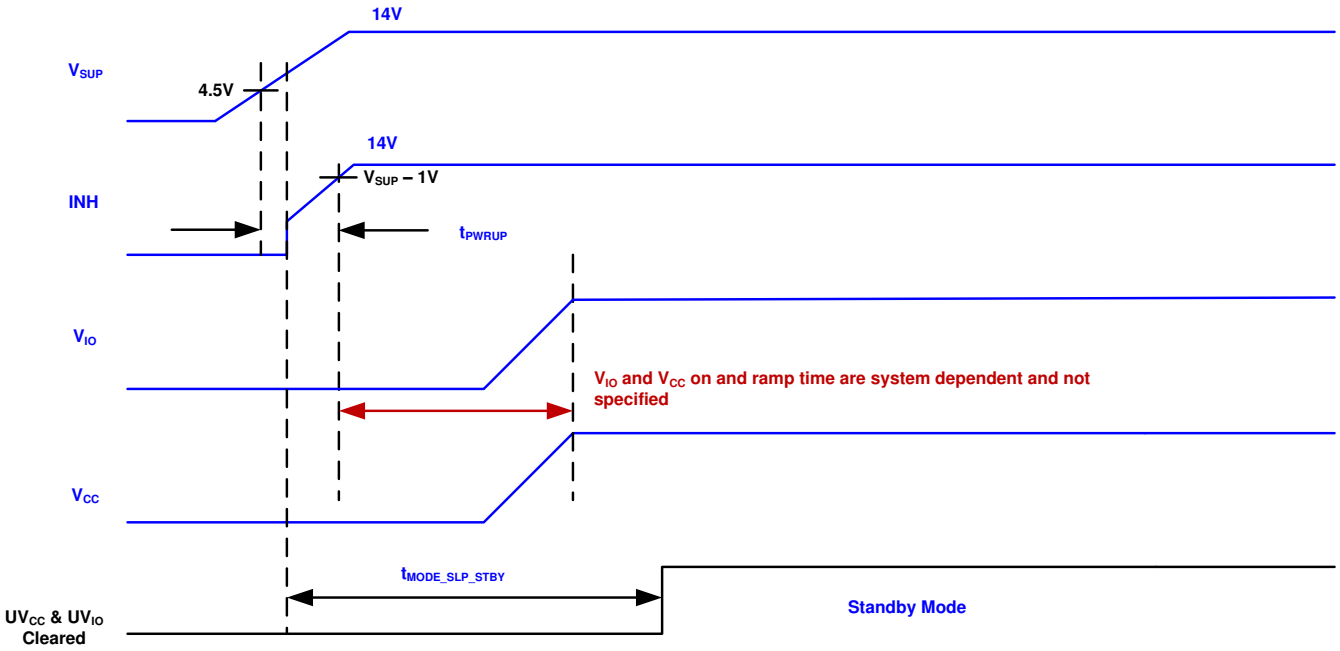


Figure 9-12. Power Up Timing

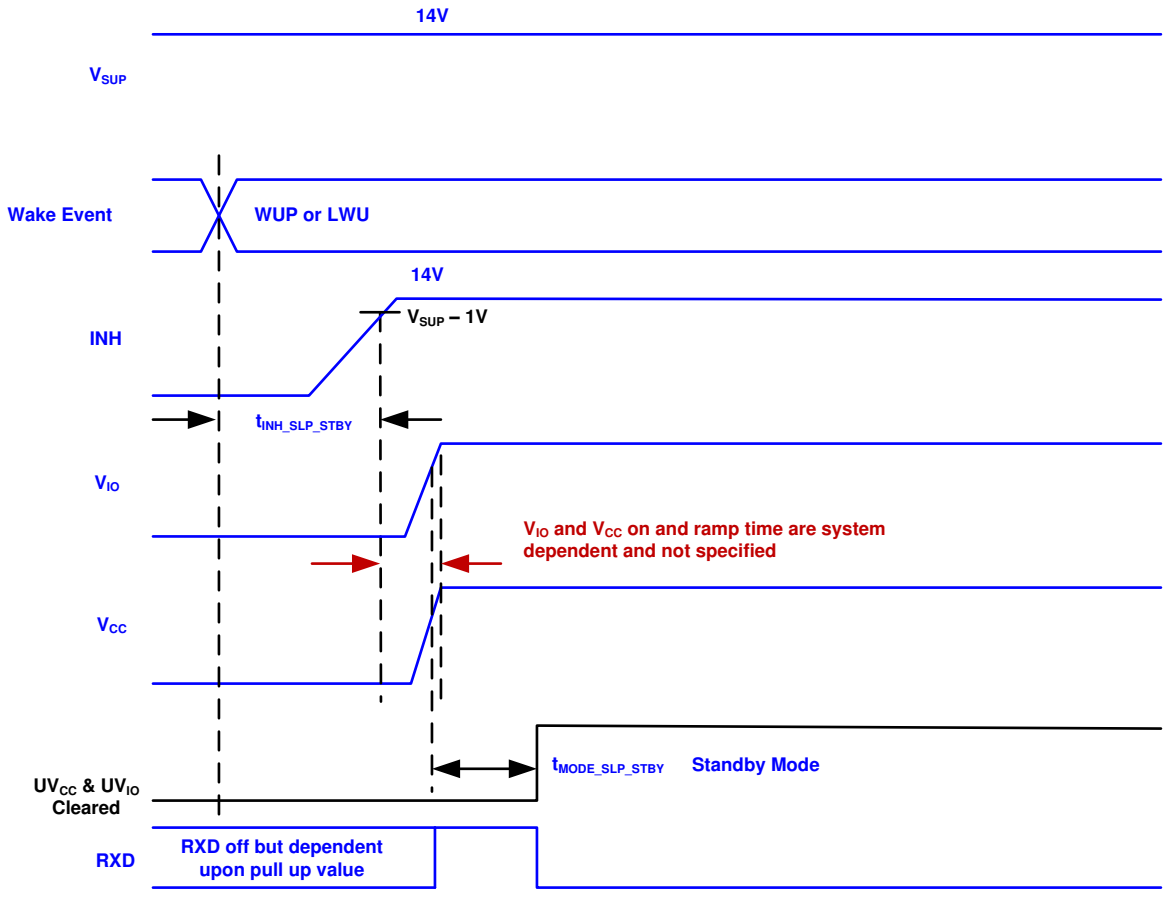


Figure 9-13. Sleep to Standby Timing

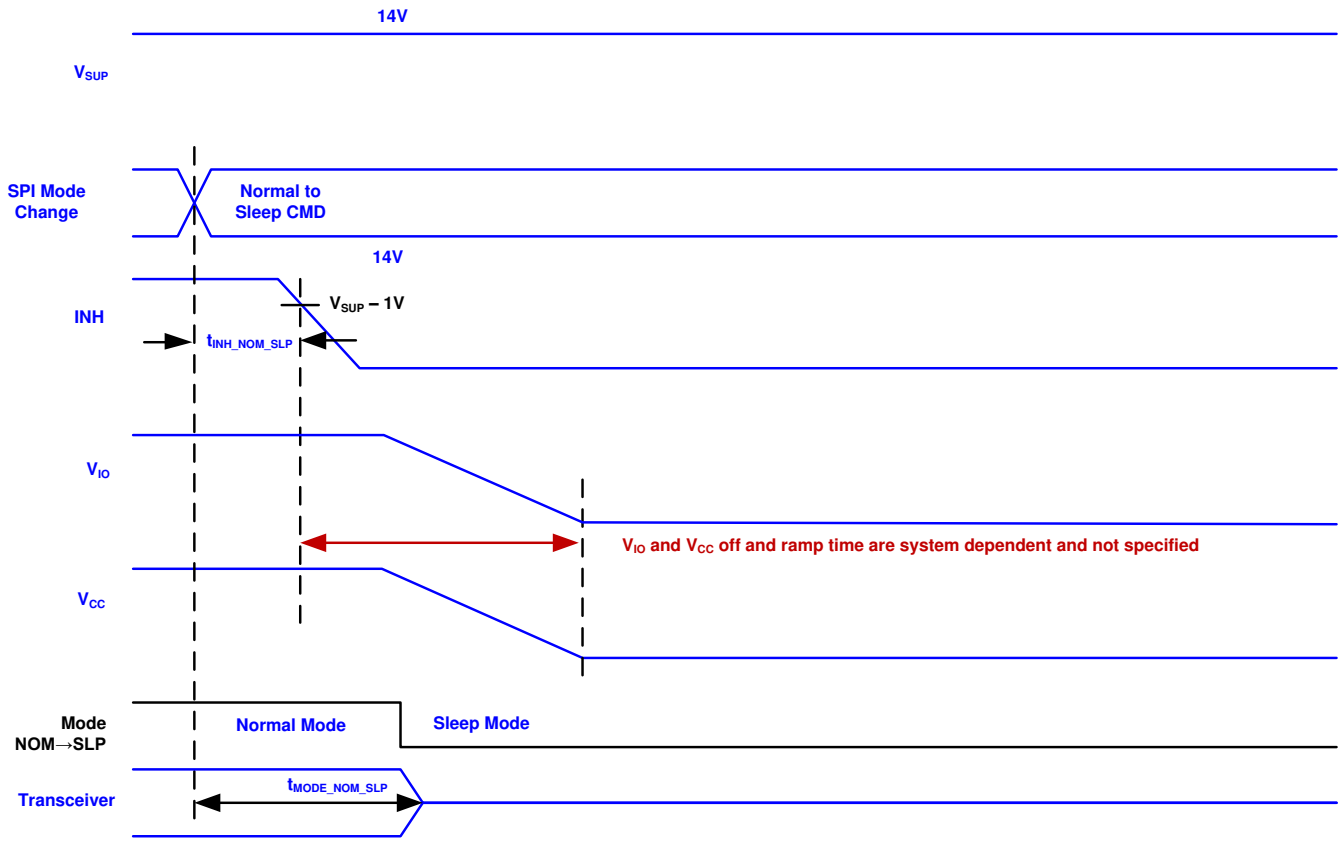


Figure 9-14. Normal to Sleep Timing

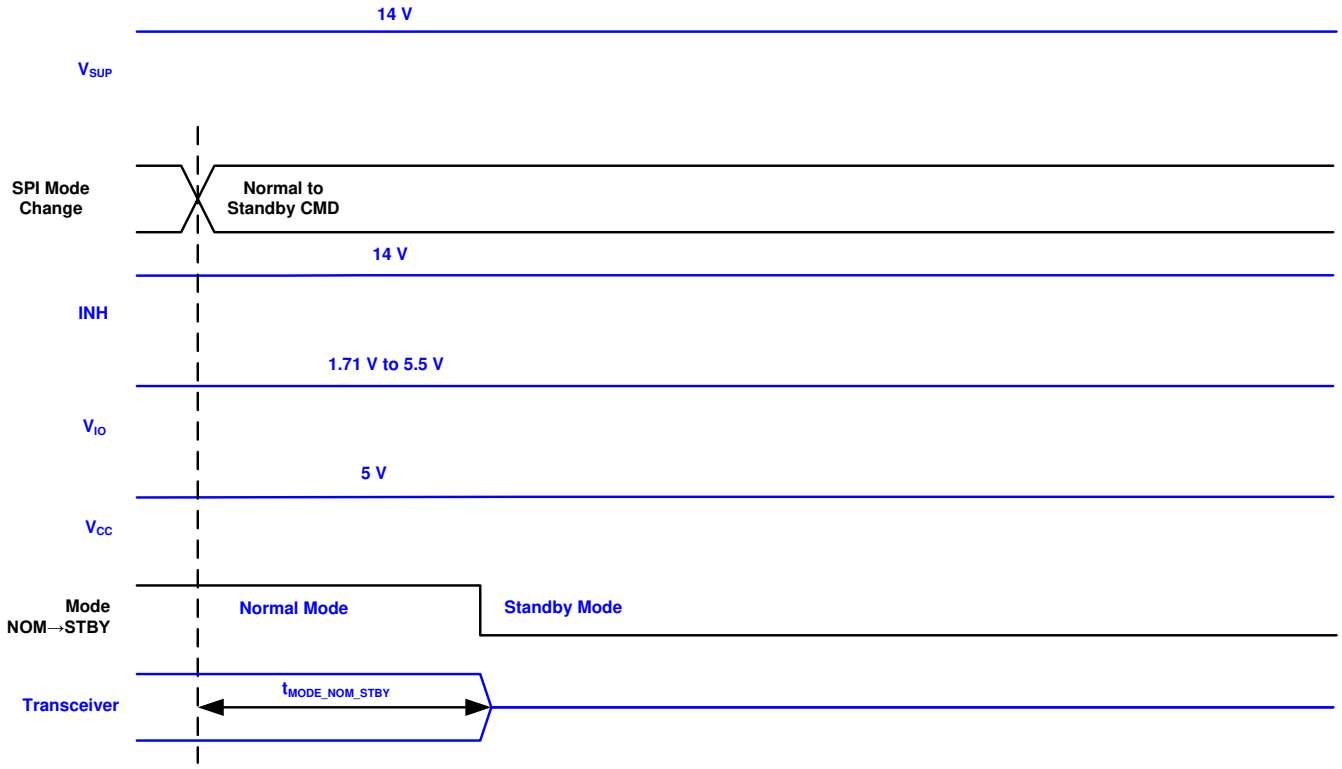


Figure 9-15. Normal to Standby Timing

Note

The blue signals are input or output of the TCAN114x-Q1 and the black signals are internal to the TCAN114x-Q1. This is for timing diagrams Figure 9-12, Figure 9-13, Figure 9-14 and Figure 9-15.

10 Detailed Description

10.1 Overview

The TCAN114x-Q1 is a CAN FD transceiver supporting data rates up to 5 Mbps meeting the high-speed CAN physical layer standards: ISO 11898-2:2016. The TCAN1145-Q1 and TCAN1146-Q1 support selective wake up on dedicated CAN-frames. The devices can also wake up via remote wake up using CAN bus implementing the ISO 11898-2:2016 Wake Up Pattern (WUP). The TCAN114x-Q1 supports 1.8 V, 3.3 V and 5 V processors using V_{IO} pin. The processor interface is through the SPI, RXD and TXD terminals. The devices have a Serial Peripheral Interface (SPI) that connects to a local microprocessor for configuration. SPI supports clock rates up to 4 MHz. The serial data output (SDO) pin can be configured as an interrupt output pin when the chip select pin is high providing flexibility for system design.

The TCAN114x-Q1 provides CAN FD transceiver function: differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features providing device and CAN network robustness.

The CAN bus has two logical states during operation: recessive and dominant. See Figure 9-1 and Figure 9-2.

Recessive bus state is when the bus is biased to a common mode of about 2.5 V via the high resistance internal input resistors of the receiver of each node on the bus across the termination resistors. Recessive is equivalent to logic high and is typically a differential voltage on the bus of almost 0 V. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes may transmit a dominant bit at the same time. In this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

Transceivers have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 9-1 and Figure 9-2.

The TCAN114x-Q1 provides many enhanced features that are provided in the Section 10.3 section. Enhanced features such as advanced bus fault detection, fail-safe, watchdog and providing a processor interrupt are described in their specific subsections.

10.2 Functional Block Diagram

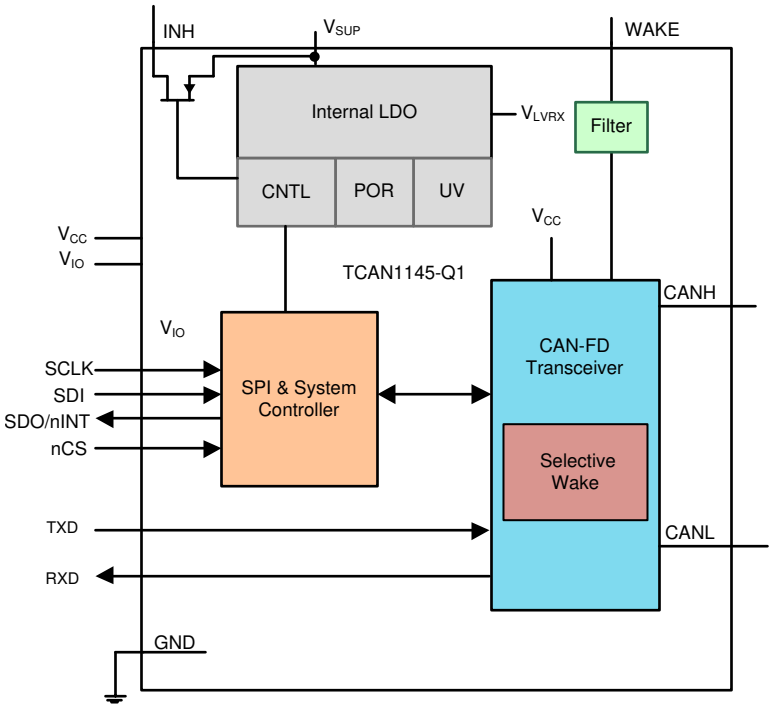


Figure 10-1. TCAN1145-Q1 Functional Block Diagram

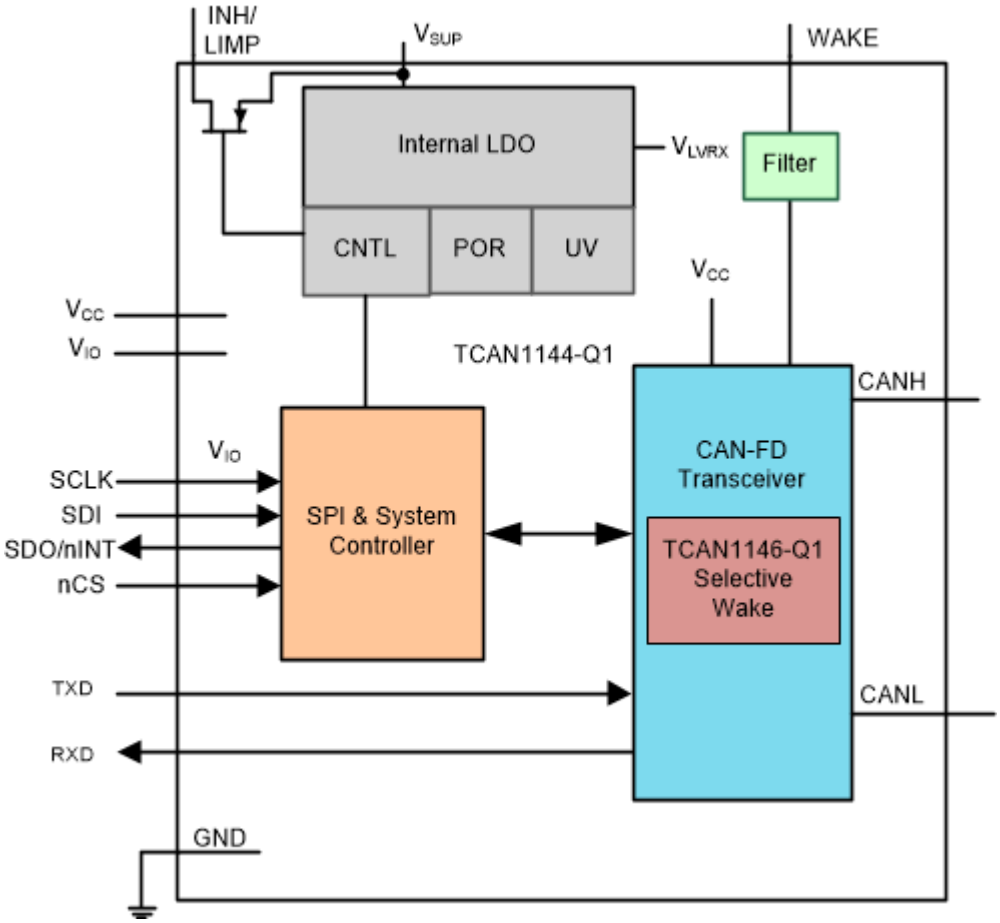


Figure 10-2. TCAN1144-Q1 and TCAN1146-Q1 Functional Block Diagram

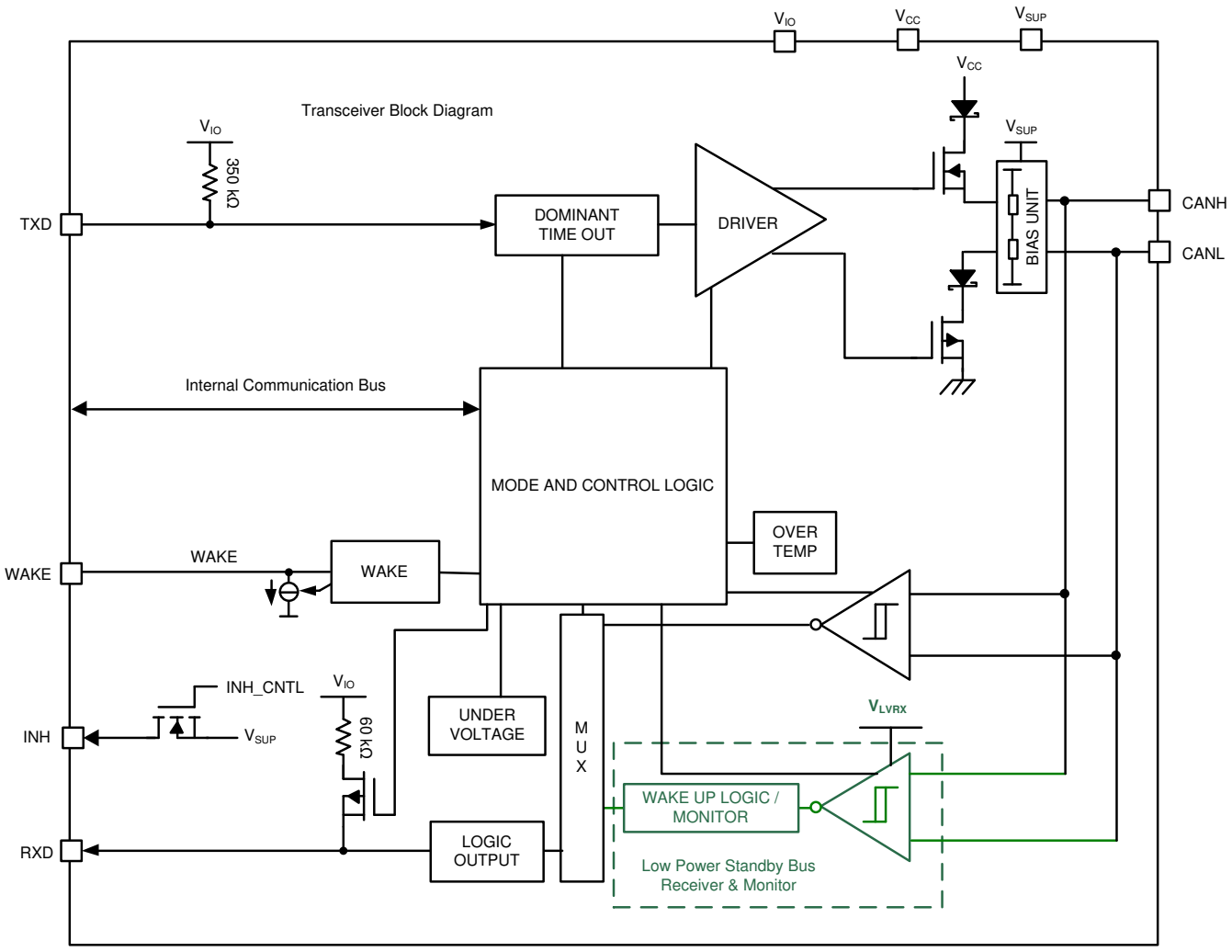


Figure 10-3. TCAN1145-Q1 CAN Transceiver Block Diagram

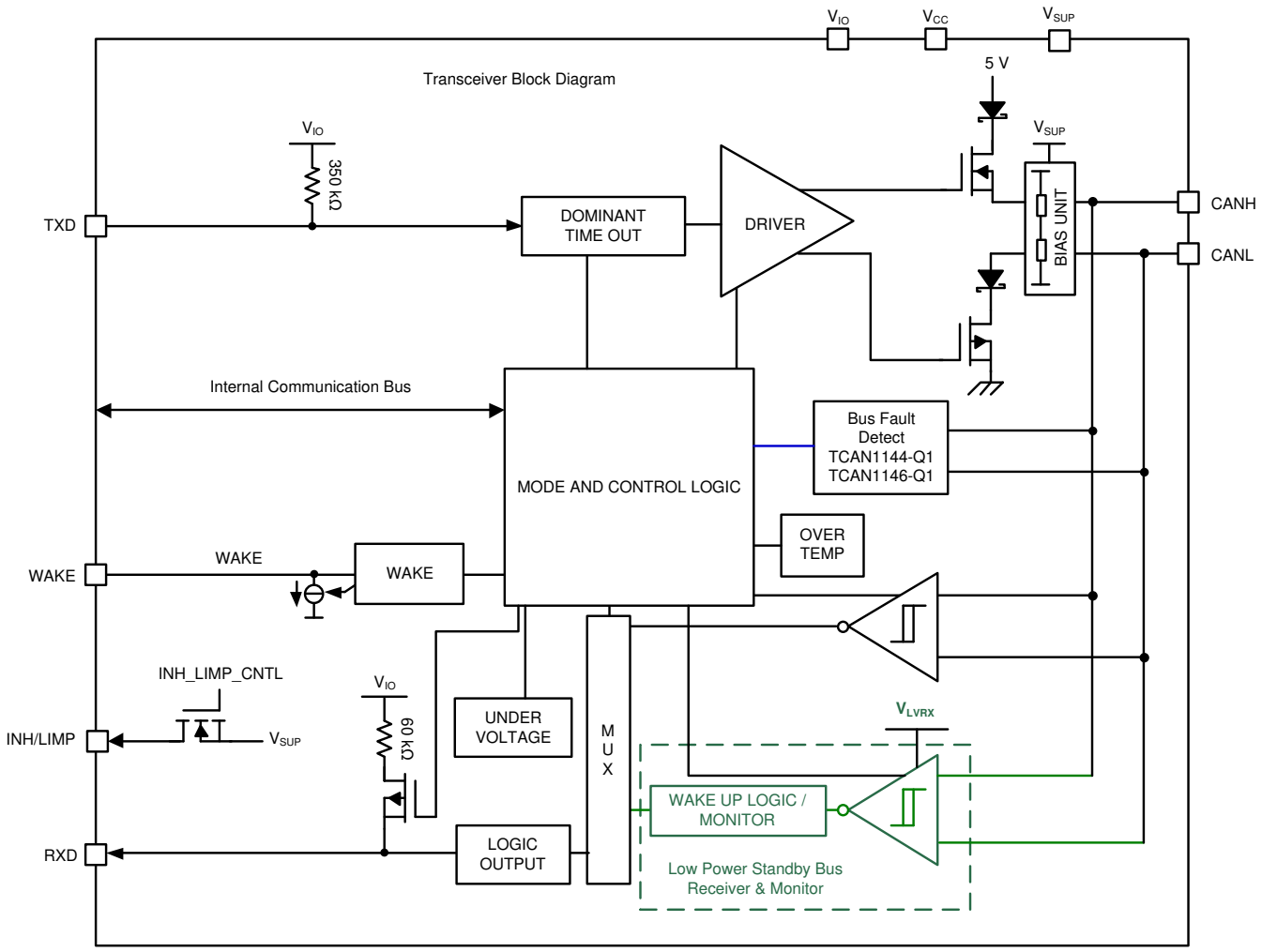


Figure 10-4. TCAN1144-Q1 and TCAN1146-Q1 CAN Transceiver Block Diagram

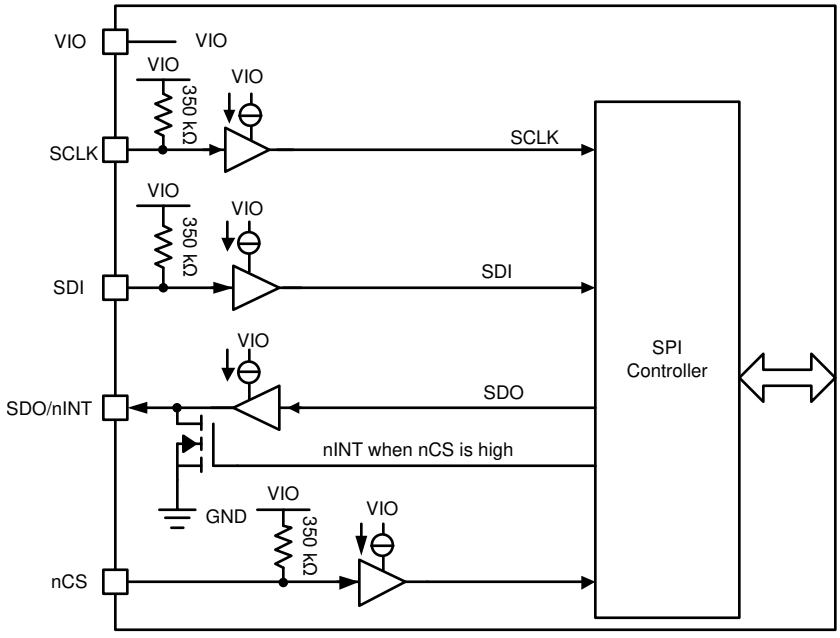


Figure 10-5. TCAN114x-Q1 SPI and Digital IO Block Diagram

10.3 Feature Description

10.3.1 V_{SUP} Pin

This pin connects to the battery supply. It provides the supply to the internal regulators that support the digital core and low power CAN receiver.

10.3.2 V_{IO} Pin

The V_{IO} pin provides the digital IO voltage to match the microprocessor IO voltage thus avoiding the requirements for a level shifter. V_{IO} supports SPI pins. The TCAN114x-Q1 family support processors with 1.8 V, 3.3 V and 5 V input/output which provides the widest range of controller support.

10.3.3 V_{CC} Pin

The V_{CC} pin provides the 5 V to the internal CAN transceiver.

10.3.4 GND

The GND pin is for ground. The thermal pad should be connected to the GND plane for heat dissipation.

10.3.5 INH/LIMP Pin

The INH pin is a high voltage output pin that provides voltage from the V_{SUP} minus a diode drop to enable an external high voltage regulator. These regulators are usually used to support the microprocessor and V_{IO} pin. The INH function is on in all modes except for sleep mode. In sleep mode the INH pin is turned off, going into a high Z state. This allows the node to be placed into the lowest power state while in sleep mode. If this function is not required it can be disabled by setting register 8'h1A[6] = 1b using the SPI interface. If this function is not required, TCAN1144-Q1 and TCAN1146-Q1 can configure this pin as a LIMP home pin by setting register 8'h1A[5] = 1b. When configured as the LIMP pin it is connected to external circuitry for a limp home mode. If the Watchdog times out, the device by default turns on the LIMP home function. To turn off LIMP three consecutive (default) correct watchdog input triggers must take place. The number of correct watchdog input triggers can be changed to one using LIMP_SEL_RESET, register 8'h1A[3:2] = 01b. If fail-safe mode is enabled, any event that causes the device to enter this mode causes the LIMP pin to turn on if LIMP is enabled. Writing a 1b to 8'h1A[1], LIMP_RESET, can be used to turn off the LIMP pin.

Note

This terminal should be considered a "high voltage logic" terminal, not a power output; thus, it should be used to drive the EN terminal of the system's power management device and not used as a switch for power management supply itself. This terminal is not reverse battery protected and thus should not be connected outside of the system module.

10.3.6 WAKE Pin

WAKE pin is used for a local wake up (LWU). This function is explained further in Section 10.4.4.2 section. The pin is defaulted to bi-directional edge trigger, meaning it recognizes a local wake up (LWU) on either a rising or falling edge of WAKE pin transition. This default value can be change via a SPI command that either configures it as a rising edge only, a falling edge only, a pulse of specific width and timing or a filtered rising or falling edge. This is done by using register 8'h11[7:0]. Pin requires a 22 nF capacitor to ground between the two resistors.

10.3.7 TXD Pin

The TXD pin is an input from the processor for the CAN bus.

10.3.8 RXD Pin

The RXD pin is the output to the processor from the CAN bus. When a wake event takes place, this pin is pulled low by default. The wake-up action can be changed to pulse by setting register 8'h12[2] = 1b, RXD_WK_CONFIG. Upon power up, the RXD pin is pulled low as the device has entered standby mode. The RXD pin has an internal 60 kΩ pull-up to V_{IO} that is active when $V_{SUP} \leq UV_{SUP}$, POR or when the device is in sleep mode.

10.3.9 SDO/nINT Interrupt Pin

The nINT shares the pin with the SPI serial data output (SDO) function and is defaulted as SDO only. If the pin is to be used as nINT, register 8'h29[0] should be set to 1b, SDO_CONFIG. When configured to support nINT, the pin functions as an interrupt output when the nCS pin is high and by default is pulled low for a global interrupt, 8'h50[7:0]. When nCS is low the device is using the SPI ports and this pin is the serial data output from the TCAN114x-Q1. Figures Figure 10-6 and Figure 10-7 show an example high level system and timing diagram when using the nINT feature.

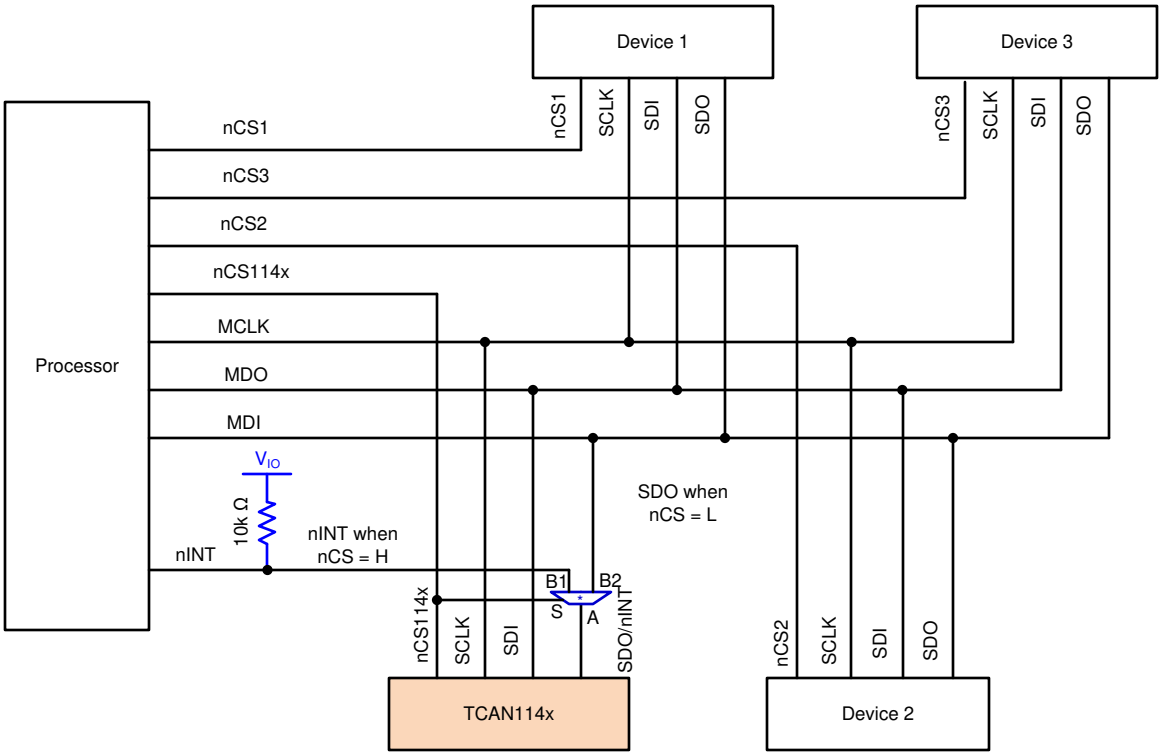
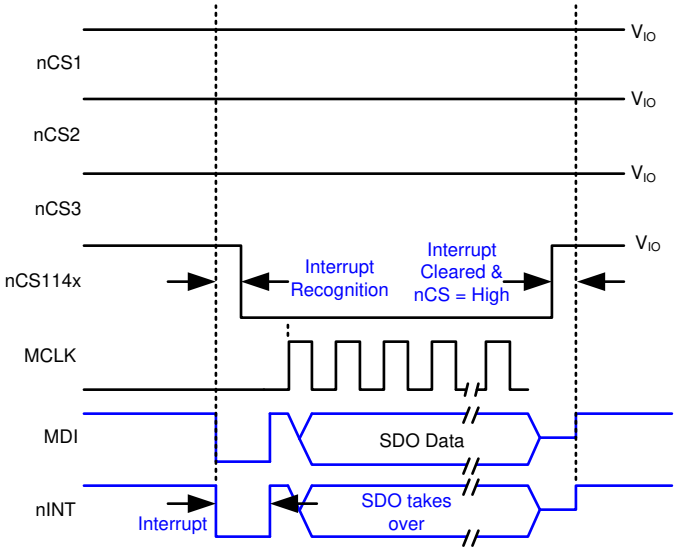


Figure 10-6. Example System Using nINT Feature



* This shows an interrupt and how SDO would behave
* Device recognizes nCS pulled low and releases nINT function for SDO
* See SPI section for overall SPI bus timing

Figure 10-7. nINT Timing Diagram

Note

- To use the nINT feature a point to point architecture for the SPI bus is recommended but not required.
- When using the nINT feature in a multidrop system it is recommended that before communicating with another device on the SPI bus the first step is to disable this feature and then re-enable after communication has stopped. This avoids an interrupt from corrupting the SDO line.
- The nINT is the logical OR of all faults in registers 8'h50 to 8'h54 that are not masked.

10.3.10 nCS Pin

The nCS pin is the SPI chip select pin. When pulled low and a clock is present the device can be written to or read from.

10.3.11 SCLK

The SCLK pin is the SPI clock to the TCAN114x-Q1. The max clock rate is 4 MHz.

10.3.12 SDI

When nCS is low this pin is the SPI serial data input pin used for programming the device or requesting data.

10.3.13 CANH and CANL Bus Pins

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low voltage WUP CAN receiver. The functionality of these is explained throughout the document. See Section 11.1.2.2 for CAN bus biasing.

10.4 Device Functional Modes

The TCAN114x-Q1 has several operating modes: normal, standby, listen, sleep and fail-safe mode and two protected modes. The first four mode selections are made by the SPI register, 8h10[2:0]. Fail-safe mode if enabled is entered due to various fault conditions. The protected modes are a modified standby modes used to protect the device or bus when fail-safe mode is disabled. The TCAN114x-Q1 automatically goes from sleep to standby mode when receiving a WUP or LWU event. When selective wake is enabled, TCAN1145-Q1 and TCAN1146-Q1, the device looks for a wake-up frame (WUF) after receiving a WUP. If a WUF is not received the device transitions back to sleep mode. See Table 10-1 for the various modes and what parts of the device are active during each mode.

The TCAN114x-Q1 state diagram figure, see Figure 10-8, Figure 10-9 and Figure 10-10 which show the biasing of the CAN bus in each of the modes of operation.

Table 10-1. Mode Overview

Block	Normal	Standby	Listen	Sleep	Fail-safe	UV_{IO} Protected	TSD Protected (Fail-safe Disabled)
nINT (If Enabled)	On	On	On	Off	Fault Determines	Off	On
INH	On	On	On	Off	On	On	On
LIMP (If Enabled): TCAN1144-Q1 TCAN1146-Q1	Off unless WD fail	Off	Off	Off	On if Enabled	Off	Off
WAKE	Off	On	Off	On	See Note	Off	Off
SPI	On	On	On	On if VIO present	Fault Determines	Off	On
Watchdog: TCAN1144-Q1 TCAN1146-Q1	On	On	Off	Off	Off	Off	Off
Low Power CAN RX	Off	On	Off	On	On	On	On
CAN Transmitter	On	Off	Off	Off	Off	Off	Off
CAN Receiver	On	Off	On	Off	Off	Off	Off

Note

Fail-safe mode has several blocks that state Fault Determines. The following provides an explanation.

- nINT and SPI can be active if the fault condition is UV_{CC} or TSD. These blocks are off if the fault condition is UV_{IO}.
- INH (default) in fail-safe mode is on, so the processor has power and can read which fault has occurred. When using the fail-safe counter after programmed number of wake up and go back to fail-safe cycles INH can be programmed to turn off and then on.
- The low power CAN (WUP) receiver is powered off of V_{SUP}. A UV_{SUP} event will cause this receiver to be off.
- Once the fail-safe counter limit has been reached and if register 8'h17[6:4] = 100b, FS_CNTR_ACT, the device will enter sleep mode and not respond to wake request. A hard reset (power cycle) is required to bring the device back to normal operation.
- In fail-safe mode the SWE timer starts and wake events are ignored until the fault is cleared. Once fault is cleared the WAKE pin is active.
  - If the SWE timer times out the device will enter Sleep mode. This can happen even if faults are cleared and if no wake event has taken place or the device hasn't had SPI communication like changing modes.

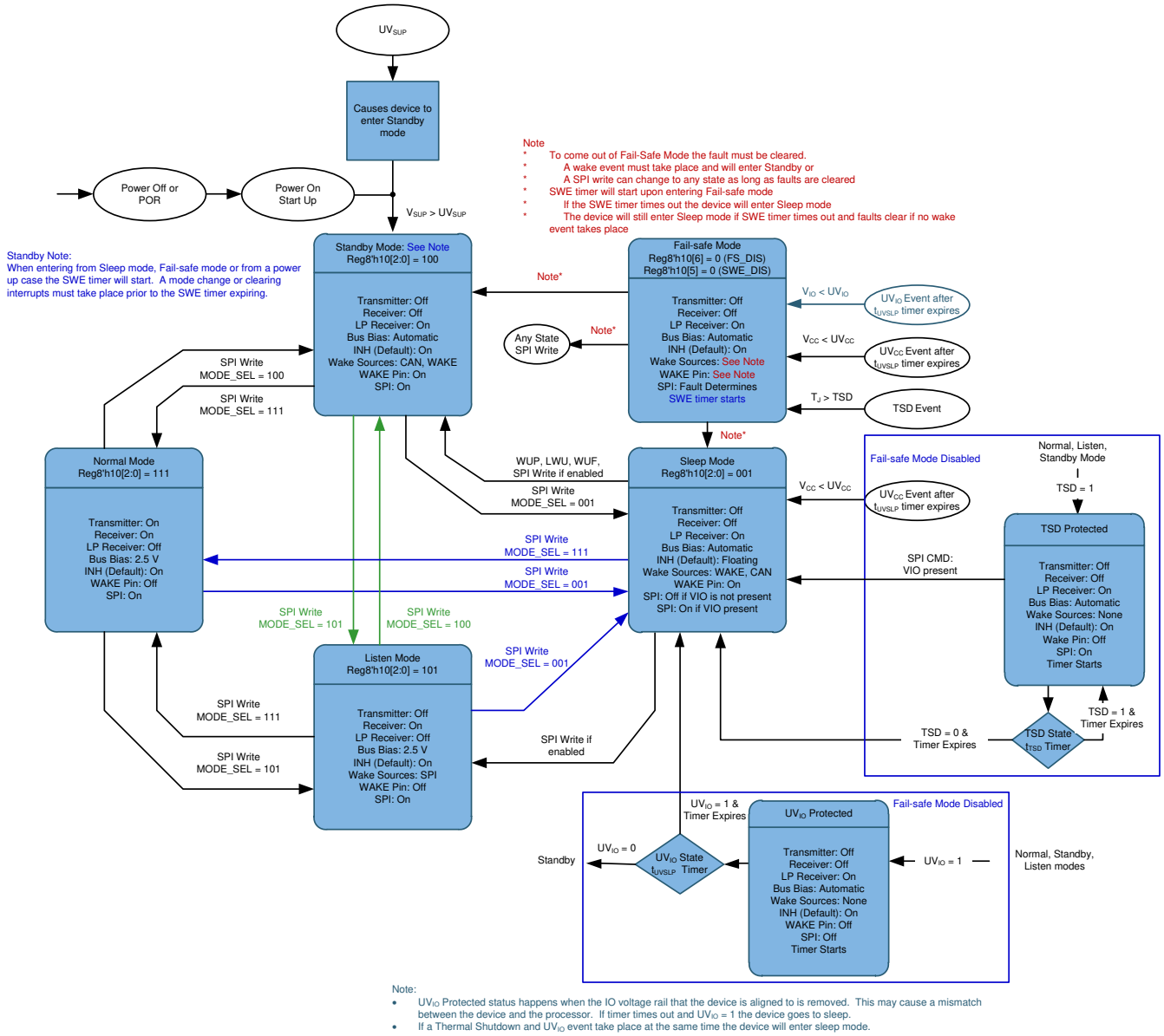


Figure 10-8. TCAN1145-Q1 Device State Diagram

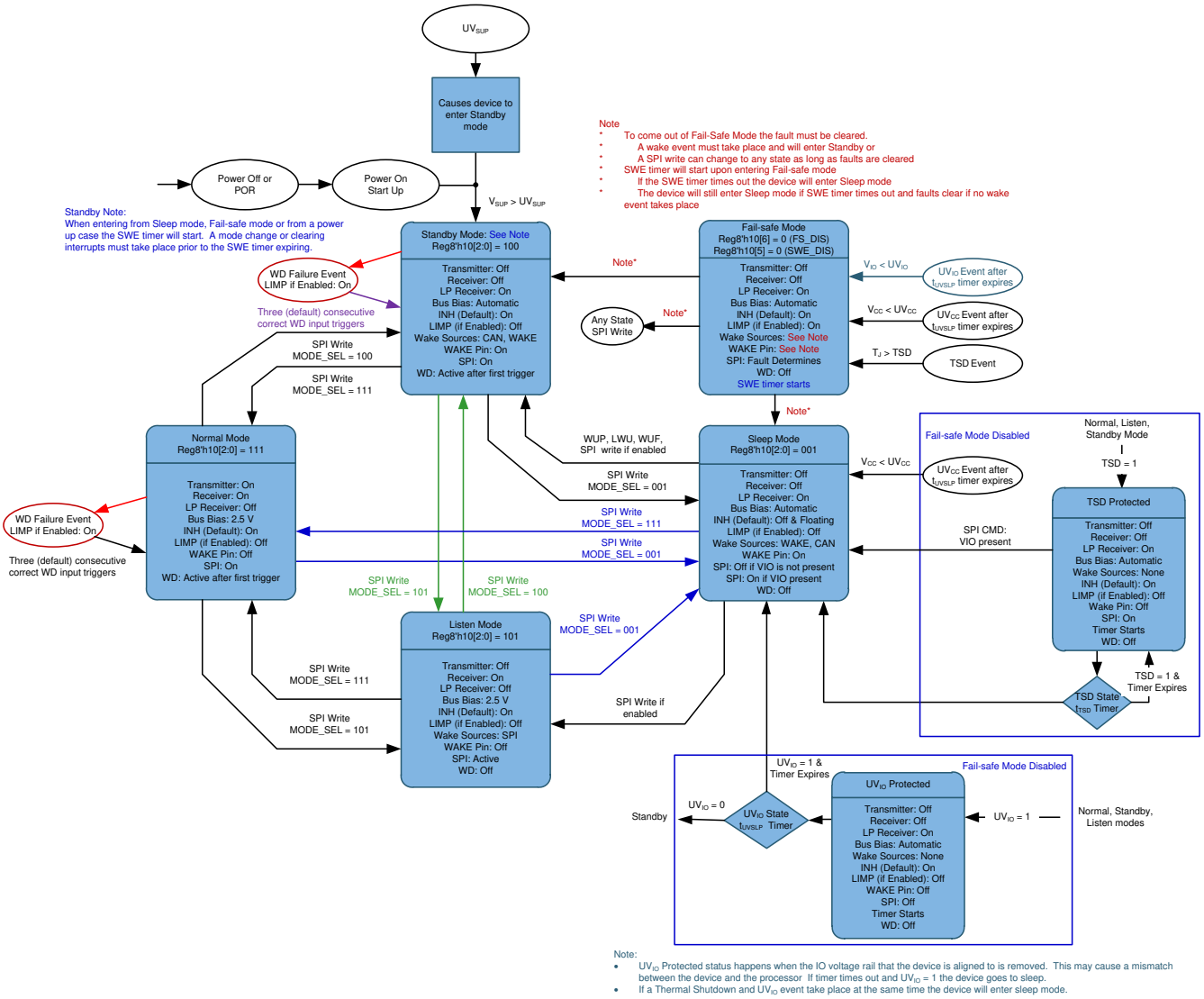


Figure 10-9. TCAN1146-Q1 Device State Diagram

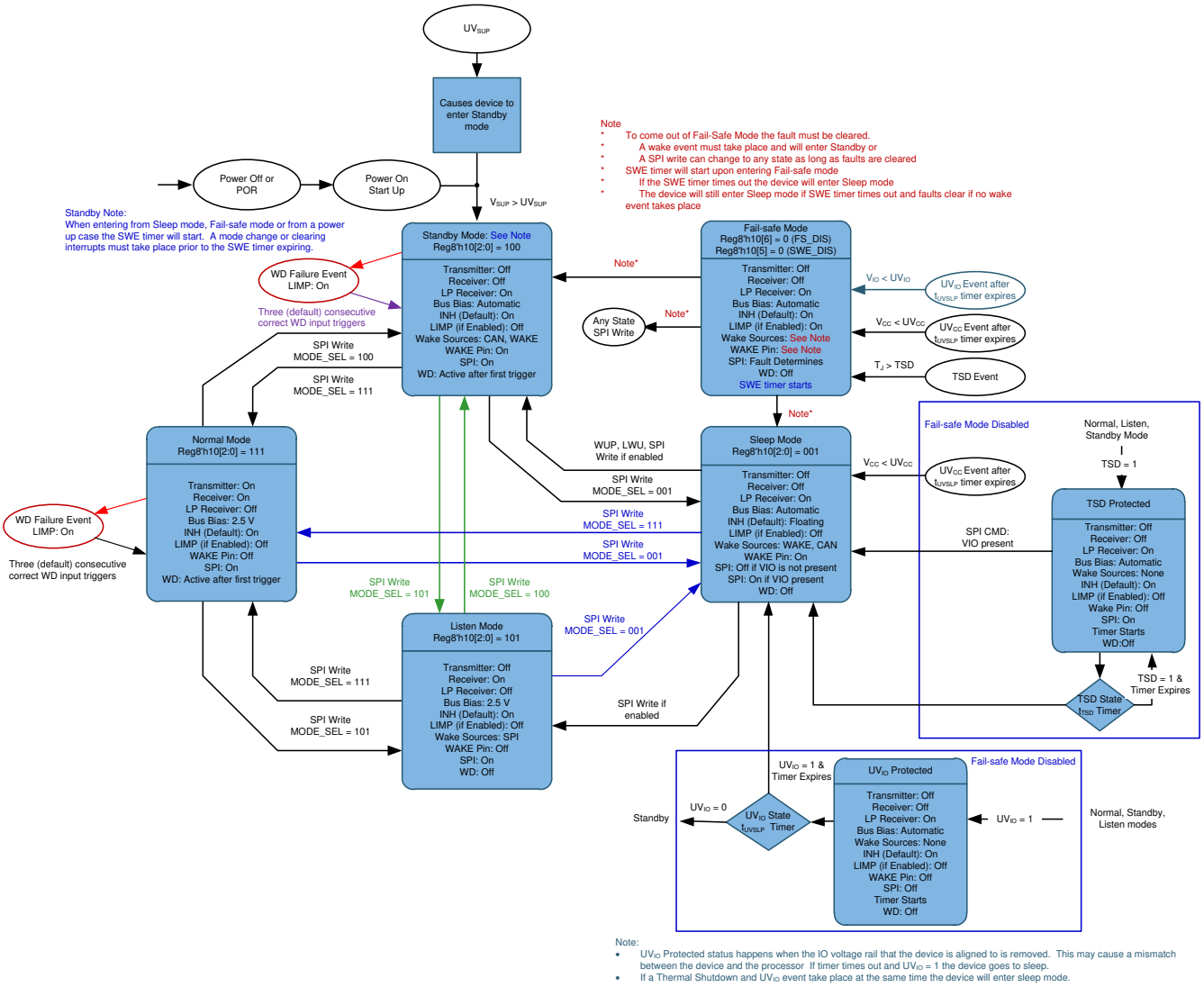


Figure 10-10. TCAN1144-Q1 Device State Diagram

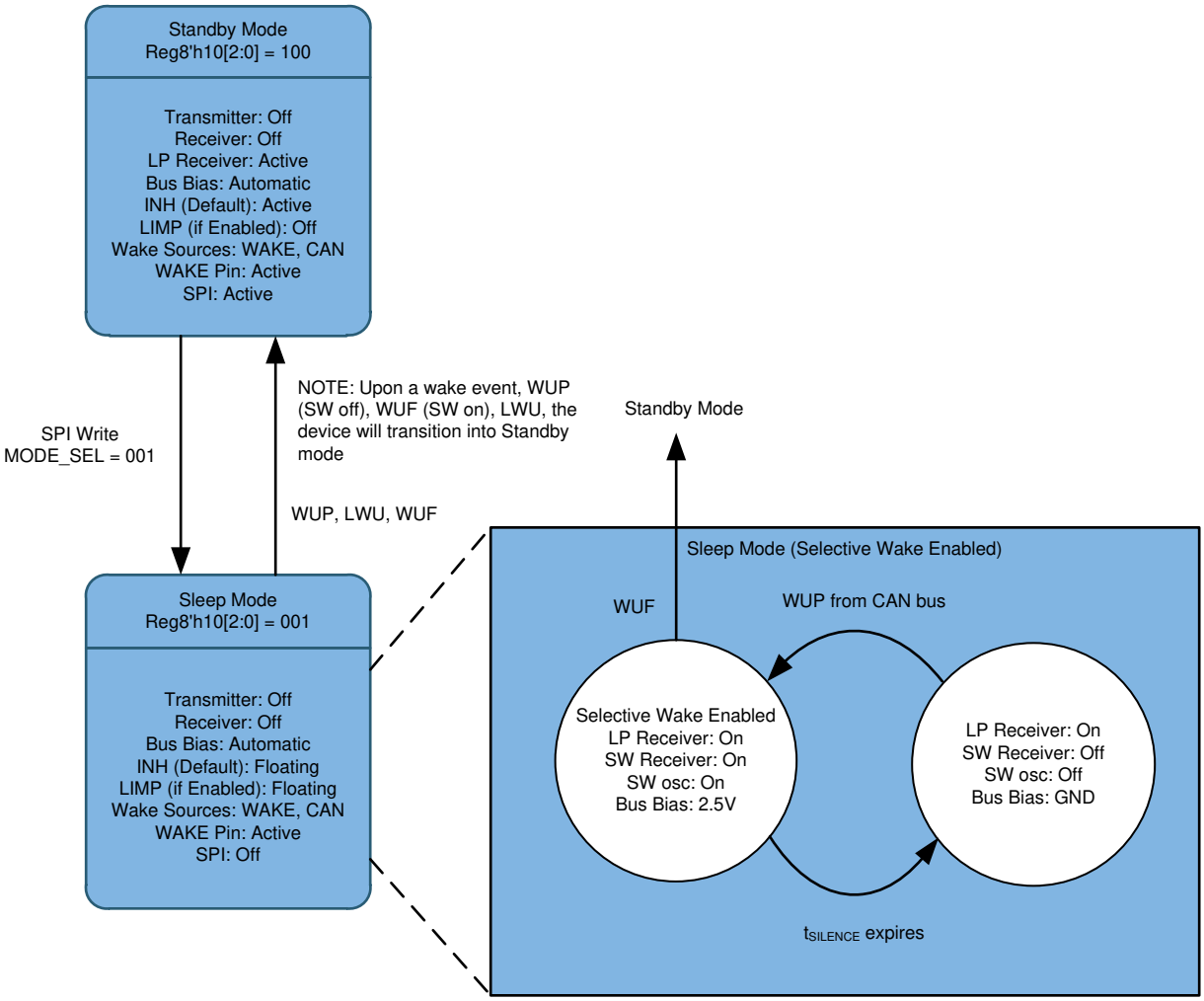


Figure 10-11. TCAN1145-Q1 and TCAN1146-Q1 Selective Wake Enabled Sleep Mode

Note

For the state diagrams by default SPI is off in sleep mode. If V_{IO} is present SPI will work in sleep mode but at a reduced data rate, which would include selective wake sub state as shown in Figure 10-11.

10.4.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD signal from the CAN FD controller to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD signal to the CAN FD controller. Normal mode is enabled or disabled via SPI interface.

When fail-safe mode and the SWE timer are enabled a SPI command to enter normal mode will turn off the SWE timer. It is recommended to clear any interrupts in the process. There are two cases that will cause the SWE timer to start while in normal mode.

- CANSLNT_SWE_DIS = 0 which starts the SWE timer after CANSLNT interrupt is set. CANSLNT interrupt needs to be cleared to stop the timer.
- CANSLNT_SWE_DIS = 1 (default) which starts the SWE timer when no bus activity is present for longer than $t_{SILENCE}$. Bus activity will clear $t_{SILENCE}$ timer reset the SWE timer.

When the SWE timer times out the device will enter sleep mode.

10.4.2 Standby Mode

In standby mode, the bus transmitter does not send data nor does the normal mode receiver accept data. There are several blocks that are active in this mode. The low power CAN receiver is actively monitoring the bus for the wake-up pattern (WUP). The WAKE pin monitor is active. The SPI interface is active so that the microprocessor can read and write registers in the memory for status and configuration. The INH pin is active in order to supply an enable to the V_{IO} controller if this function is used. The device goes from sleep mode to standby mode automatically upon a bus WUP event, WUF event or a local wake up from the WAKE pin. If V_{IO} is present the device can wake up from a SPI mode change command.

Upon power up, a power on reset or wake event from sleep mode the TCAN114x-Q1 enters standby mode. This starts the SWE timer, $t_{INACTIVE}$, that requires the processor to either reset the interrupt flags or configure the device to normal or listen modes. This feature makes sure the node will be in the lowest power mode if the processor does not come up properly. This automatic mode change also takes place when the device has been put into sleep mode and receives a wake event, WUP, WUF or LWU. To disable this feature for sleep events, register 8'h1C[7] (SWE_DIS) must be set to one. This does not disable the feature when powering up or when a power on reset takes place.

The following provides the description on how selective wake interacts between sleep and standby modes for TCAN1145-Q1 and TCAN1146-Q1.

- At power up, the device is in standby. Clear all Wake flags (PWRON, WUP/LWU), configured the Selective Wake registers, and then set selective wake config (SWCFG = 1) and selective wake enable (SW_EN = 1).
- When SWCFG = 1 and the device is placed into sleep mode the low power WUP receiver is active and waiting for a WUP.
- Once a WUP is received the WUF receiver is active.
- The device receives the wake-up frame and determines if the node has been requested to wake up.
  - If the WUF is a valid match, the device wakes up the node entering standby mode.
  - If the WUF is not a valid match, the device stays in sleep mode.
- A wake interrupt occurs from any type – WUF (CANINT), FRAME_OVF or LWU (if enabled), the device enters standby mode.

Note

When in standby mode the RXD pin will be released back to high when the PWRON, LWU, CANINT and FRAME_OVF interrupts have been cleared.

10.4.3 Listen Only Mode

In this mode, the CAN transmitter is disabled with only the receiver enabled. Data on the CAN bus is seen on the RXD pin but anything on the TXD does not reach the CAN bus. All other functionality is the same as Normal Mode except for Watchdog is off. When fail-safe mode and SWE timer is enabled the same behavior as provided in normal mode is present in listen only mode.

10.4.4 Sleep Mode

Sleep mode is similar to the standby mode except the SPI interface and INH typically are disabled. As the low power CAN receiver is powered off of V_{SUP} the implementer can turn off V_{IO}. If V_{IO} is present in sleep mode, SPI access can take place but at a reduced rate. If at least a 10 µs delay is used between pulling nCS low and the start of a read or write the max SPI rate can be utilized. If V_{IO} is off, the SPI interface is turned off and the only ways to exit sleep mode is by a wake-up event or power cycle. A sleep mode status flag is provided to determine if the device entered sleep mode through normal operation or if a fault caused the mode change. Register 8'h52[7] provides the status. If a fault causes the device to enter sleep mode, this flag is set to a one.

Note

Difference between Sleep and Standby Mode

- Sleep mode reduces whole node power by shutting off INH to the VREG enable pin and thus shutting off power to the node.
- Standby mode reduces TCAN114x-Q1 power from Normal mode but has higher power than Sleep mode, as INH is enabled, turning on node processors VREG. SPI interface is active.

10.4.4.1 Bus Wake via RXD Request (BWRR) in Sleep Mode

The TCAN114x-Q1 supports low power sleep and standby modes and uses a wake up from the CAN bus mechanism called bus wake via RXD Request (BWRR). Once this pattern is received, the TCAN114x-Q1 automatically switches to standby mode from sleep mode and inserts an interrupt onto the nINT pin, if enabled, to indicate to a host microprocessor that the bus is active, and the processor should wake up and service the TCAN114x-Q1. The low power receiver and bus monitor are enabled in sleep mode to allow for RXD Wake Requests via the CAN bus. A wake-up request is output to the RXD (driven low) as shown in Figure 10-12. The external CAN FD controller monitors RXD for transitions (high to low) and reactivates the device to normal mode based on the RXD Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, prior to BWRR if $t_{SILENCE}$ is expired, see Figure 9-2.

This device uses the wake-up pattern (WUP) from ISO 11898-2: 2016 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the RXD terminal (BWRR).

The wake-up pattern (WUP) consists of

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the RXD pin. The behavior of this pin is determined by register h'12[2]. If h'12[2] = 0 the RXD pin is pulled low once the WUP pattern has been received that meets the dominant, recessive, dominant filtered times. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP and transition to BWRR output.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no BWRR is generated.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a BWRR may be generated.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP; thus, a BWRR is always generated.

See Figure 10-12 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and a bus stuck dominant fault from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under voltage event occurs on V_{CC} the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time; otherwise, the device is in a state waiting for the next recessive and then a valid WUP pattern.

If h'12[2] = 1 the RXD pin toggles low to high to low for t_{TOGGLE} = 10 µs until the device is put into normal or listen mode. BWRR is active in standby mode upon power up and once coming out of sleep mode or certain fail-safe mode conditions. If a SPI write puts the device into standby mode, the RXD pin is high until a wake event takes place. The RXD pin then behaves like it would when waking up from sleep mode.

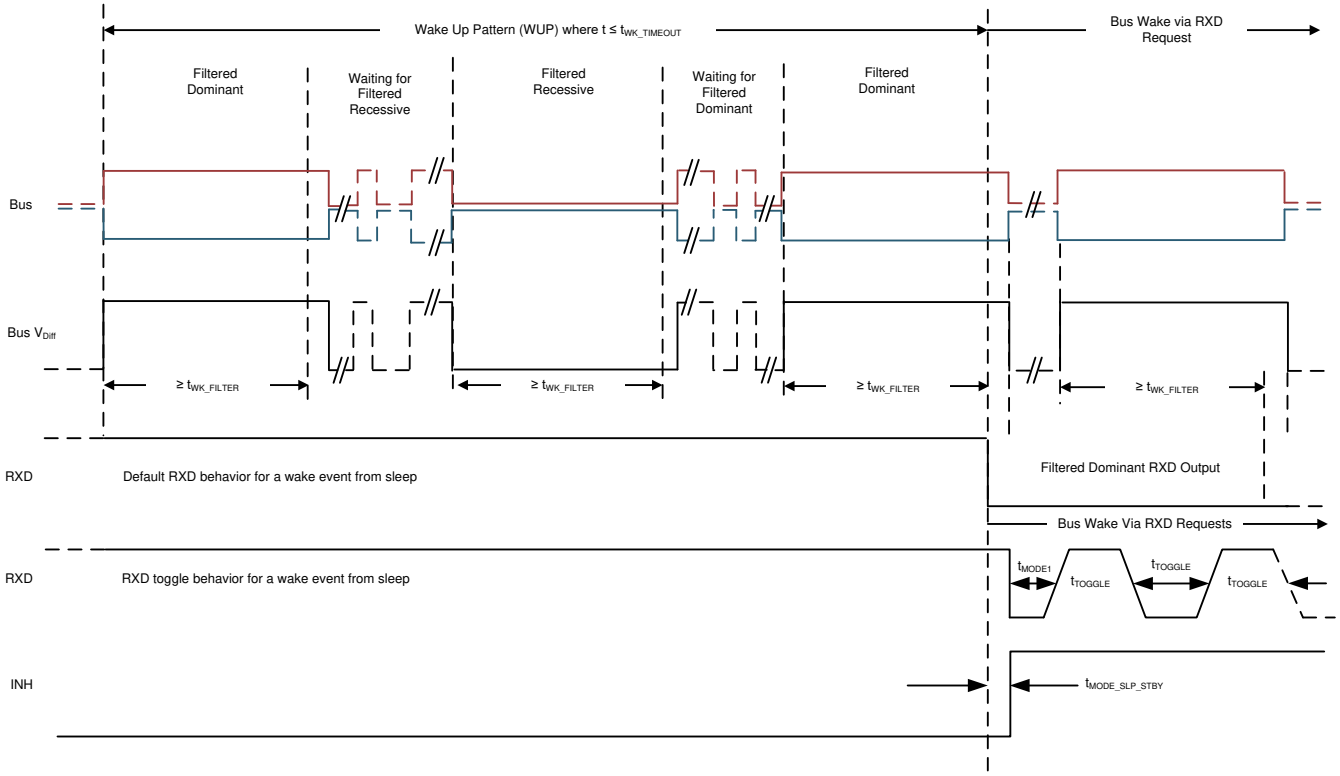


Figure 10-12. Wake Up Pattern (WUP) and Bus Wake via RXD Request (BWRR)

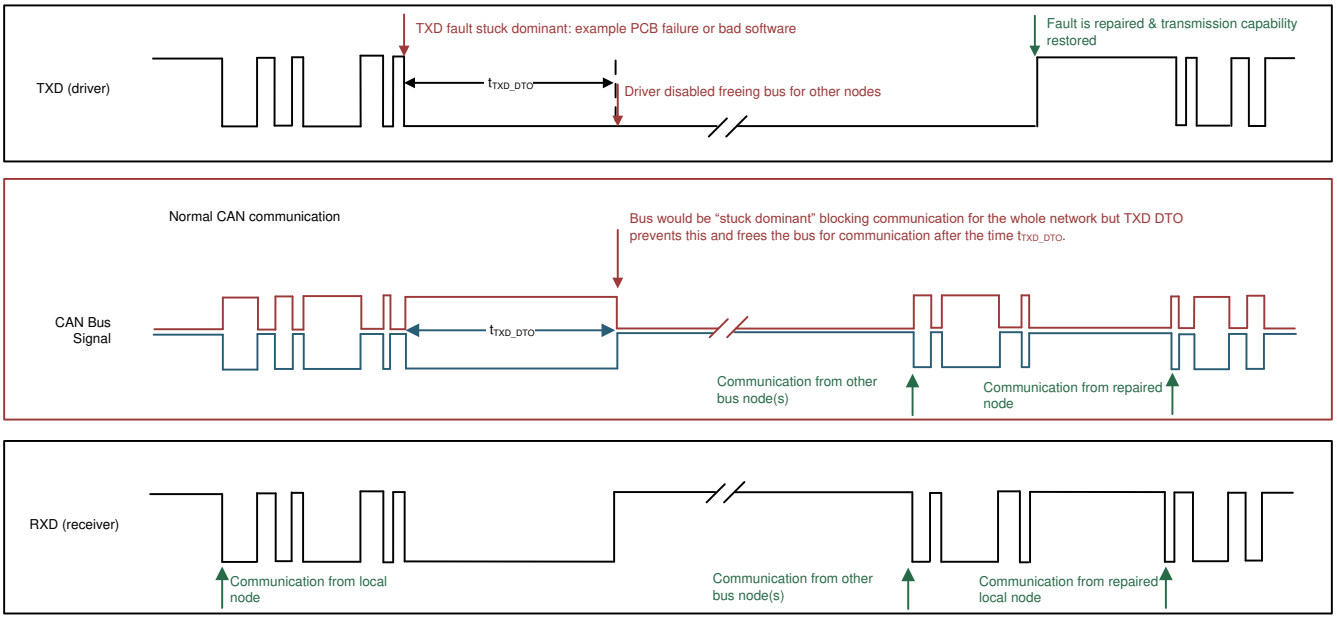


Figure 10-13. Example timing diagram with TXD DTO

10.4.4.2 Local Wake Up (LWU) via WAKE Input Terminal

The WAKE terminal is a ground biased input terminal that can support high voltage wake inputs used for local wake up (LWU) request via a voltage transition. The terminal triggers a LWU event on either a low to high or high to low transition as it has bi-directional input thresholds. This terminal may be used with a switch to V_{SUP} or ground. If the terminal is not used it should be pulled to ground to avoid unwanted parasitic wake up events.

The WAKE terminal defaults to bi-directional input but can be configured for rising edge and falling edge transitions, see Figure 10-14 and Figure 10-15, by using WAKE_CONFIG register 11h[7:6]. Once the device enters sleep mode the WAKE terminal voltage level needs to be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input can be determined.

There are two other wake methods that can be utilized with the WAKE pin, a pulse wake and a filtered wake. For the pulsed wake input a pulse on the WAKE pin must be within a specified time to be considered valid. A pulse width less than $t_{WAKE\_INVALID}$ will be filtered out for both the pulse and filtered wake configurations. For the pulse configuration, the pulse must be between $t_{WK\_WIDTH\_MIN}$ and $t_{WK\_WIDTH\_MAX}$, see Figure 10-16. This figure provides three examples of pulses and whether the device will wake or not wake. $t_{WK\_WIDTH\_MIN}$ is determined by the value for $t_{WK\_WIDTH\_INVALID}$ which is set by register 11h[3:2]. There are two regions where a pulse may or may not be detected. By using register 1Bh[1], WAKE_WIDTH_MAX_DIS, the pulse mode can be configured as a filtered wake input. Writing a 1 to this bit will disable $t_{WK\_WIDTH\_MAX}$ and the WAKE input will be based upon the configuration of register 11h[3:2] which selects a $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$ value. A WAKE input of less than $t_{WK\_WIDTH\_INVALID}$ will be filtered out and if longer than $t_{WK\_WIDTH\_MIN}$ INH will turn on and device will enter standby mode. The region between the two may or may not be recognized, see Figure 10-17. Register 12h[7] determines the direction of the pulse or filter edge that is recognized. The status of the WAKE pin can be determined from register 11h[5:4]. When a WAKE pin change takes place, the device will register this as a rising edge or falling edge. This will be latched until a 00 is written to the bits.

The LWU circuitry is active in sleep mode, standby mode and transition state of going to sleep. If a valid LWU event occurs the device transitions to standby mode. The LWU circuitry is not active in normal mode. A constant high level on WAKE has an internal pull up to V_{SUP}, and a constant low level on WAKE has an internal pull down to GND. On power up this may look like a LWU event and could be flagged as such.

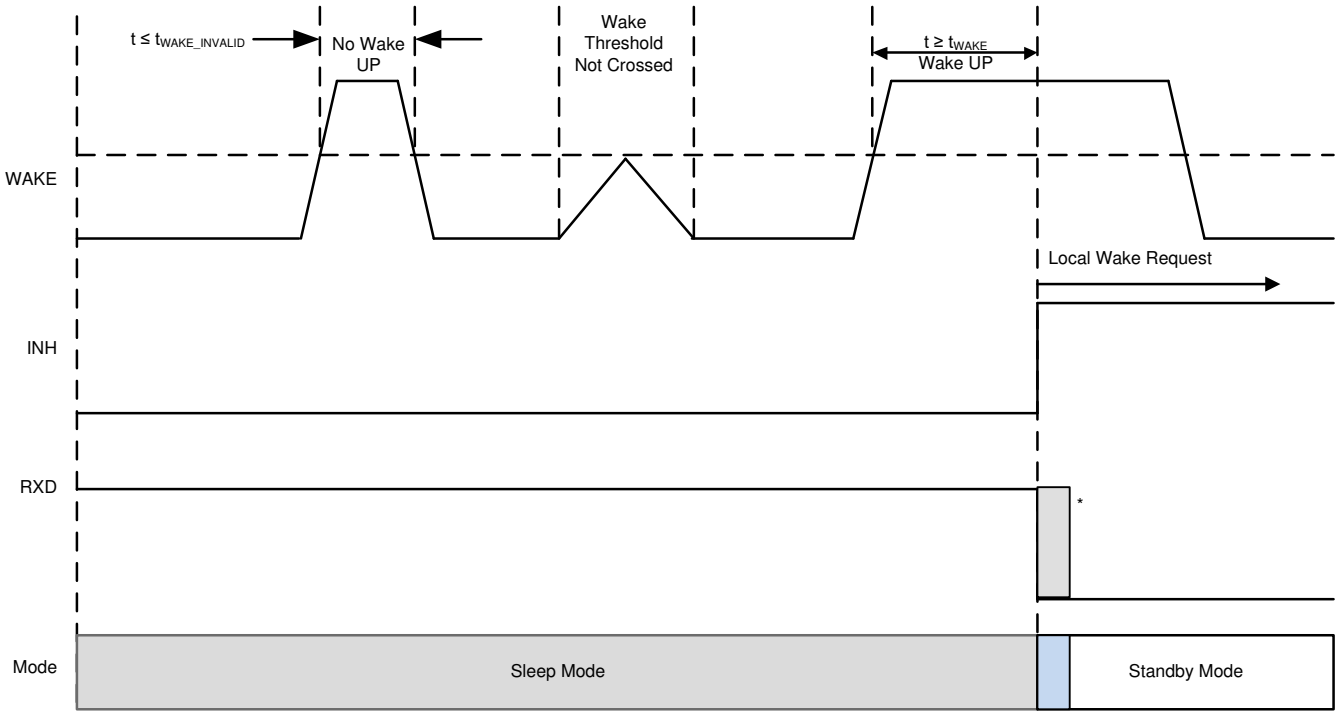


Figure 10-14. Local Wake Up – Rising Edge

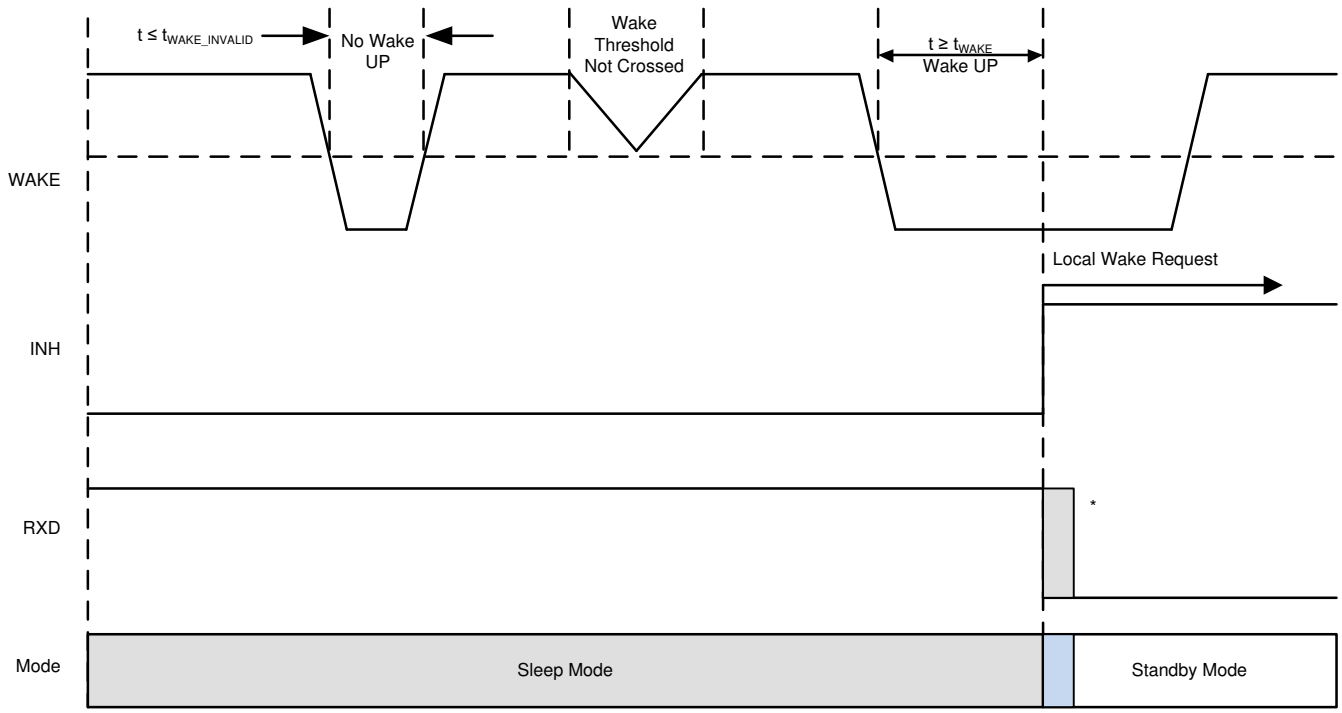


Figure 10-15. Local Wake Up – Falling Edge

Note

When either a rising or falling edge is selected for the WAKE pin the state prior to the edge requires a t_{WAKE} period of time.

- If a rising edge is selected and the device goes to sleep with WAKE high, a low of at least t_{WAKE} must be present prior to the rising edge wake event
- If a falling edge is selected and the device goes to sleep with WAKE low, a high of at least t_{WAKE} must be present prior to the falling edge wake event
- This requirement is not necessary for a bidirectional edge (default)
- Figure 10-14 and Figure 10-15 provide examples of a rising or falling edge WAKE input. t_{WAKE} is based upon the time it takes from a valid WUP to INH turning on. RXD will be pulled low once V_{IO} > UV_{IO} and V_{CC} > UV_{CC} and standby mode is entered.

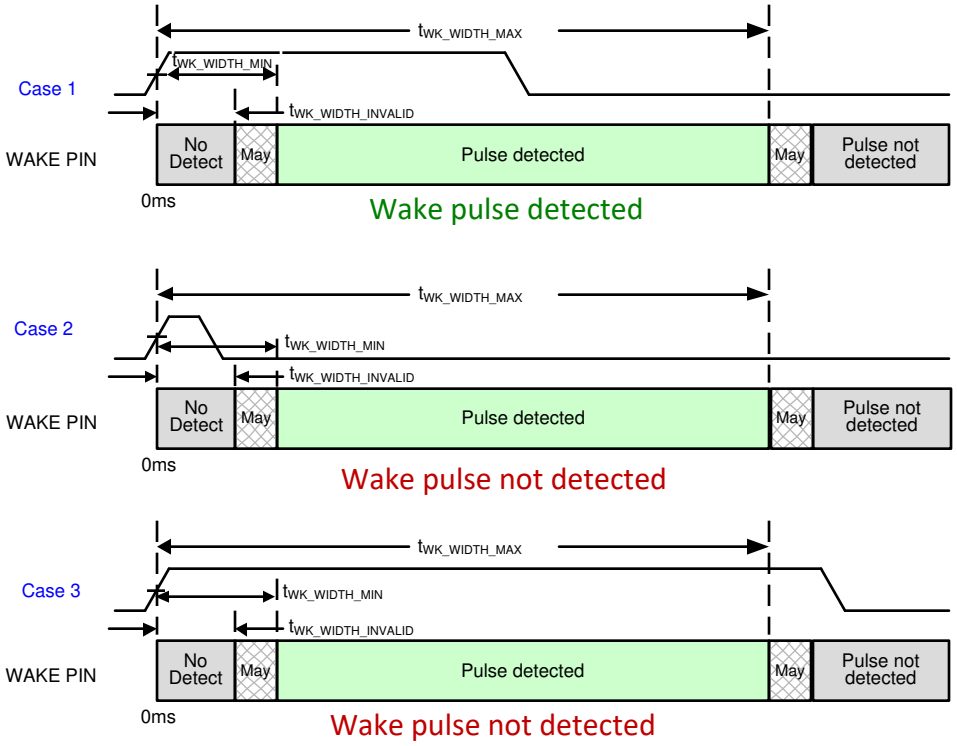


Figure 10-16. WAKE Pin Pulse Behavior

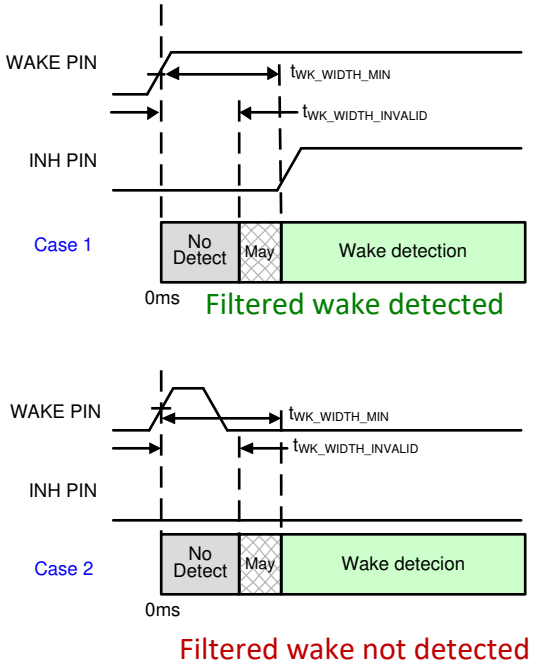


Figure 10-17. WAKE Pin Filtered Behavior

10.4.5 Selective Wake-up

The TCAN1145-Q1 and TCAN1146-Q1 supports selective wake-up according to ISO 11898-2:2016.

10.4.5.1 Selective Wake Mode (TCAN1145-Q1 and TCAN1146-Q1)

This is the medium level of power saving mode of the device. The WUF receiver is turned on and connected internally to the frame detection logic which is looking for a Wake-Up Frame (WUF) as outlined in the Frame

Detection section of the datasheet. The CAN bus data is not put on the RXD pin in this state. The device is supplied via the V_{SUP} supply coming from the system battery.

The valid wakes up sources in selective wake mode are:

- Wake Up Frame (WUF)
- WAKE pin local wake up (LWU). Event on WAKE pin must match the programmed requirements for WAKE pin in register 8'h11[7:6]
- Frame Overflow (FRAME_OVF)
- SPI command to another state

If a WUF and/or LWU event occurs, the wake request for the corresponding wake event flag (WUF and/or LWU) flag is set. At this point, an interrupt is provided to the MCU using the nINT pin if enabled and by pulling down the RXD pin.

To enter selective wake mode, the following conditions must be met:

- Selective Wake Configured, SWCFG, flag is set
  - All Selective Wake registers must be written followed by a read to ensure they are programmed correctly for the proper frame detection and selective wake configuration. Once configured, the SWCFG bit should be set to 1.
- Selective Wake Error, SWERR, flag is cleared
- Set Selective Wake Enable (SW_EN) = 1, register 8'h10[7] = 1

Note

If a fault condition or FRAME_OVF forces the device into sleep mode, fail-safe mode disabled, or into fail-safe mode SW_EN is disabled turning off selective wake function.

10.4.5.2 Frame Detection (TCAN1145-Q1 and TCAN1146-Q1)

The frame detection logic is what enables processing of serial data, or CAN frames, from the CAN bus. The device has selective wake control registers to set up the device to look for a programmed match using either the CAN ID (11 bit or 29 bit), or the CAN ID plus the data frame including data masking. If the detected CAN frame received from the bus matches the configured requirements in the frame detection logic it is called a Wake0Up Frame (WUF).

Before frame detection may be enabled or used the data needed for validation, or match, of the WUF needs to be correctly configured in the device registers. Once the device has been correctly configured to allow frame detection, or selective wake function the SWCFG (Selective Wake Configuration) must be set to load the parameters for WUF for the device. If a valid WUF is detected it is shown via the CANINT flag, including selective wake up.

When frame detection is enabled and the bus is biased to 2.5 V from a valid WUP, several other actions may take place as the logic is decoding the CAN frames the device receives on the bus. These include error detection and counting and the indication of reception of a CAN frame via the CAN_SYNC and CAN_SYNC_FD flags.

If a Frame Overflow (FRAME_OVF) occurs while in frame detection mode, it is disabled, clearing the SW_EN bit.

When frame detection is enabled transitioning from a mode where the receiver bias is not on up to four CAN frames for 500kbps and slower data rates and up to eight CAN frames for greater than 500kbps may be ignored by the device until the frame detection is stabilized.

The procedure to correctly configure the device to use frame detection and selective wake up is:

- Write all control registers for frame detection (selective wake), Selective Wake Config 1-4 (Registers 8'h44 through 8'h47), and ID and ID mask (Registers 8'h30 and 8'h40).
- Recommend reading all Selective Wake registers, allowing the software to confirm the device was written and thus configured properly.
- Set Selective Wake Configured (SWCFG) bit to 1, register 8'4F[7] = 1b.
- Set Selective Wake Enable = 1, register 8'h10[7] = 1b.

If a SWERR interrupt then occurs from the Frame Overflow flag, the Frame Overflow interrupt needs to be cleared, and then the SWCFG bit must be set again to 1.

10.4.5.3 Wake-Up Frame (WUF) Validation (TCAN1145-Q1 and TCAN1146-Q1)

When the following conditions are all met, the received frame shall be valid as a Wake-Up Frame (WUF):

- The received frame is a Classical CAN data frame when DLC (Data Length Code) matching is not disabled. The frame may also be a remote frame when DLC matching is disabled.
- The ID (as defined in ISO 11898-1:2015, 8.4.2.2) of the received Classical CAN frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID-mask illustrated in Section 10.4.5.5
- The DLC (as defined in ISO 11898-1:2015, 8.4.2.4) of the received Classical CAN data frame is exactly matching a configured DLC. See the mechanism illustrated in Section 10.4.5.6. Optionally, this DLC matching condition may be disabled by configuration in the implementation.
- When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in ISO 11898-1:2015, 8.4.2.5) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See the mechanism illustrated in Section 10.4.5.5.
- A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:2015, 10.11) is detected prior to the acknowledgment (ACK) Slot.

10.4.5.4 WUF ID Validation (TCAN1145-Q1 and TCAN1146-Q1)

The ID of the received frame matches the configured ID in all required bit positions. The relevant bit positions are determined by the configured ID in 8'h30 through 8'h33 and the programmed ID mask in 8'h34 through 8'h38. Classic Base Frame Format (CBFF) 11-bit Base ID and Classic Extended Frame Format (CEFF) 29-bit Extended ID and ID masks are supported. All masked ID bits except "do not care" must match exactly the configured ID bits for a WUF validation. If the masked ID bits are configured as "do not care" then both "1" and "0" are accepted in the ID. In the ID mask register a 1 represents “do not care”.

Figure 10-18 shows an example for valid WUF ID and corresponding ID Mask register

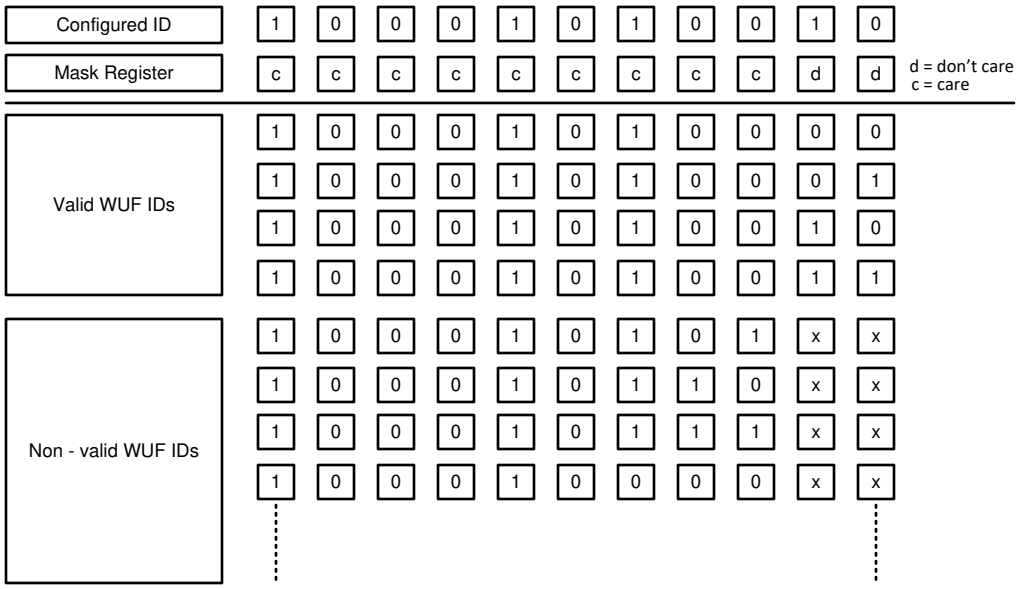


Figure 10-18. ID and ID Mask Example for WUF

10.4.5.5 WUF DLC Validation (TCAN1145-Q1 and TCAN1146-Q1)

The DLC (Data Length Code) of the received frame must match exactly the configured DLC if the data mask bit is set. The DLC is configured in 8'h38[4:1]. The data mask bit is set in 8'h38[0]. While the FD DLC are included in this table, it is important to note that selective wake only works for classic CAN frames, so CAN FD codes are not used in WUF validation.

Table 10-2. DLC

Frames	Data Length Code				Number of Data Bytes
	DLC3	DLC2	DLC1	DLC0	
Classical Frames & FD Frames	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
Classical Frames	1	0 or 1	0 or 1	0 or 1	8
FD Frames	1	0	0	1	12
	1	0	1	0	16
	1	0	1	1	20
	1	1	0	0	24
	1	1	0	1	32
	1	1	1	0	48
	1	1	1	1	64

10.4.5.6 WUF Data Validation (TCAN1145-Q1 and TCAN1146-Q1)

When the Data mask is enabled via the data mask bit, the data of the received frame must match the configured Data where at least one logic high (1) bit within the data field of the received frame matches a logic high (1) of the data field within the configured data. The relevant bit positions are determined by the configured Data in 8'h39 through 8'h40 and enabled by Data mask enable in 8'h38[0]. An example of a matching and non-matching Data is shown in Figure 10-19

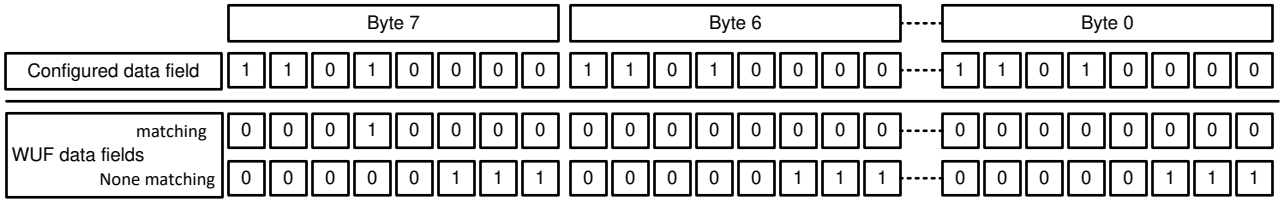


Figure 10-19. Data Field Validation for WUF Example

The selective wake data validation ensures that the last byte sent on the bus will be interpreted as data mask byte 0. This means for 8 bytes of data, the first byte sent is interpreted as data mask byte 7. For a DLC of 3, the last byte sent on the bus will be interpreted as data mask byte 0 and the first byte sent is interpreted as data mask byte 2. Below are a few examples of which bytes would be used for various bytes sent and received.

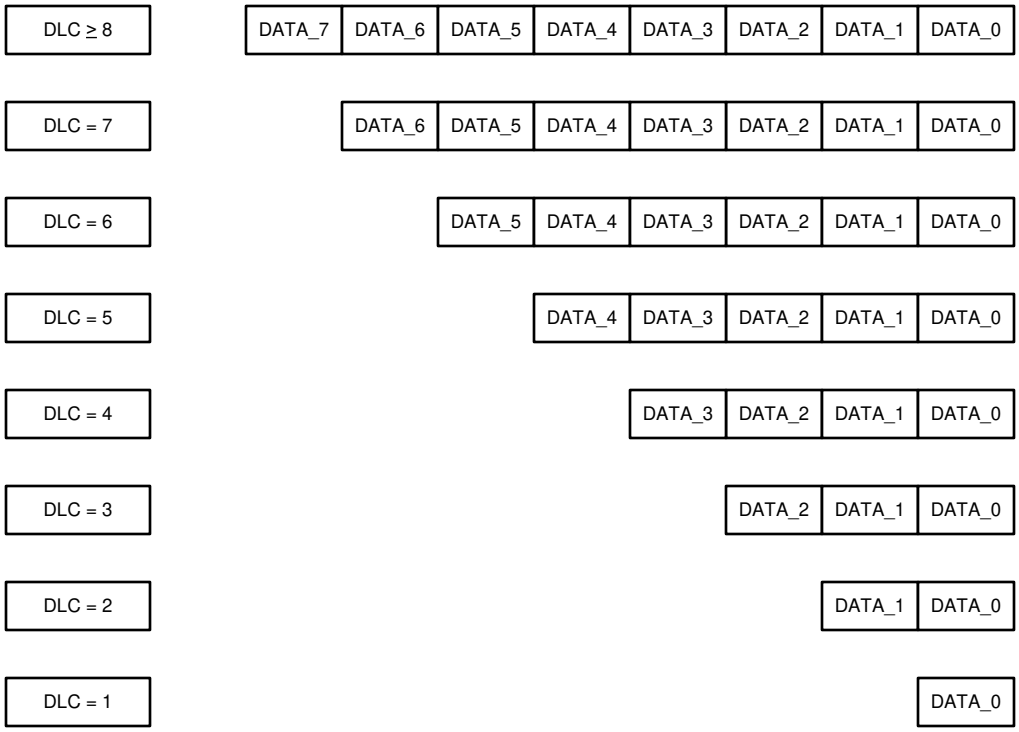


Figure 10-20. Data register mask values for different DLC values

10.4.5.7 Frame error counter (TCAN1145-Q1 and TCAN1146-Q1)

Upon activation of the selective wake up function and upon the expiration of $t_{SILENCE}$ the CAN frame error counter is set to zero. This error counter determines the CAN frame errors detected by the device. The error counter is at 8'h45 and is called FRAME_CNTx.

The initial counter value is zero and is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. If the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If a valid Classical CAN frame has been received and the counter is not zero the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field do not increase the frame error counter.

On each increment or decrement of the error counter, the decoder unit waits for nBits_idle recessive bits before considering a dominant bit as a start of frame (SOF). See Figure 10-21 for the position of the mandatory start of frame detection when classic CAN frame was received and in case of error scenario.

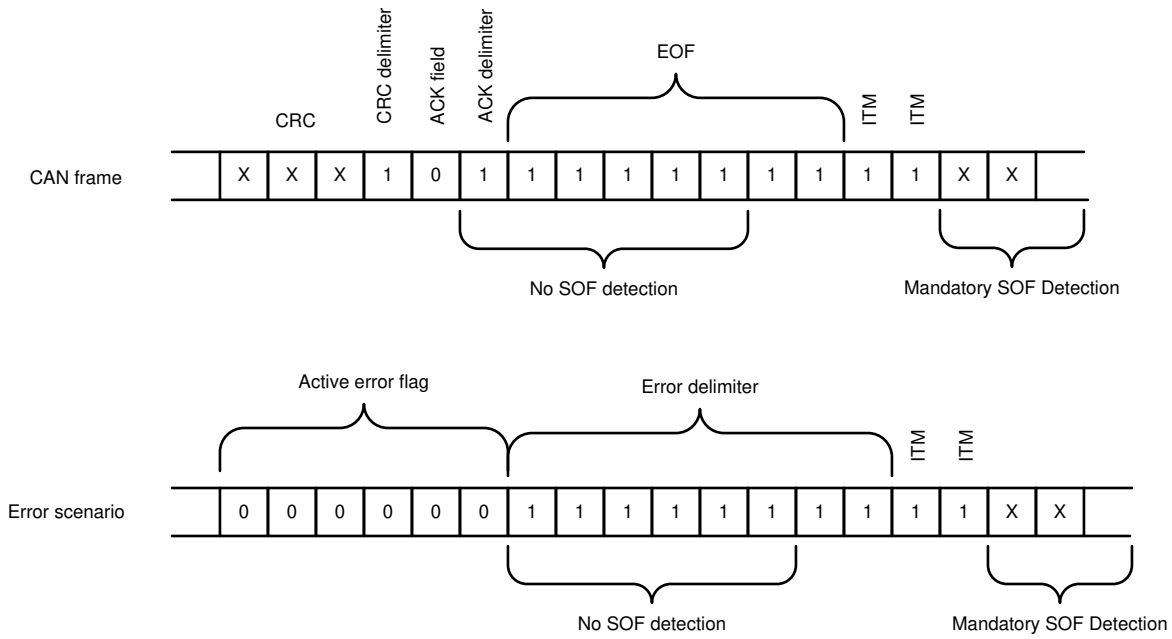


Figure 10-21. Mandatory SOF Detection after Classic CAN Frames and Error Scenarios

The default value for the frame error counter threshold is 31, so that on the 32nd error, the frame overflow flag (FRAME_OVF) is set.

When the WUP is sent, the CAN bus will bias to a recessive level, activating the WUF receiver. Up to four (or eight when bit rate > 500 kbps) consecutive Classic CAN data and/or remote frames that start after the bias reaction time, t_{Bias}, has elapsed might be either ignored, no error counter increase of failure, or judged as erroneous (error counter increases even in case of no error).

Received frames in CEFF with non-nominal reserved bits (SRR, r0) dp not lead to an increase of the error counter.

The frame error counter is compared to the frame error counter threshold, FRAME_CNT_THRESHOLD in 8'h46. If the counter overflows the threshold the frame error overflow flag, FRAME_OVF, is set. The default value for the frame error counter threshold is 31 so that on the 32nd error the overflow flag is set. However, if the application requires a different frame error count overflow threshold the required value may be programmed into the FRAME_CNT_THRESHOLD register.

The counter is reset by the following: disabling the frame detection, CANSLNT flag set, and setting register 8'h46 = 1.

The description for the errors detected:

- **Stuff bit error:** A stuff bit error is detected when the 6th consecutive bit of the same state (level) is received. CAN message coding should have had a stuff bit at this bit position in the data stream.
- **CRC error:** The CRC sequence consists of the result of the CRC calculation by the transmitting node. This device calculates the CRC with the same polynomial as the transmitting node. A CRC error is detected if the calculated result is not the same as the result received in the CRC sequence.
- **CRC delimiter error:** The CRC delimiter error is detected when a bit of the wrong state (logic low / dominant) is received in the CRC delimiter bit position which is defined as logic high (recessive).

10.4.5.8 CAN FD Frame Tolerance (TCAN1145-Q1 and TCAN1146-Q1)

After receiving a FD Format indicator (FDF) followed by a dominant res bit, the decoder unit waits for n_{Bits_idle} recessive bits before considering a further dominant bit as a SOF as per Figure 10-21. Table 10-3 defines n_{Bits_idle}.

Table 10-3. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
Number of recessive bits before a new SOF is accepted	n_{Bits_idle}	6	10

There are two bitfilter options available to support different combinations of arbitration and data phase bit rates. Register 8'h47[4] is where the $p_{Bitfilter}$ option is selected.

- Bitfilter 1: A data phase bit rate ≤ four times the arbitration rate or 2 Mbps whichever is lower shall be supported
- Bitfilter 2: A data phase bit rate ≤ ten times the arbitration rate or 5 Mbps whichever is lower shall be supported

Dominant signals ≤ the minimum pBitfilter, see Table 10-4, of the arbitration bit time in duration is not considered valid and does not restart the recessive bit counter. Dominant signals ≥ the maximum of pBitfilter of the arbitration bit time duration restart the recessive bit counter.

Table 10-4. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
CAN FD data phase bitfilter 1	pBitfilter1	5.00%	17.50%
CAN FD data phase bitfilter 2	pBitfilter2	2.50%	8.75%

10.4.6 Fail-safe Features

The TCAN114x-Q1 has fail-safe features that can be used to reduce node power consumption for a node system issue. This can be separated into two operation modes, sleep and fail-safe.

10.4.6.1 Sleep Mode via Sleep Wake Error

The sleep wake error (SWE) timer is a timer used to determine if specific external and internal functions are working. Figure 10-22 provides an overview of when SWE timer is on and starts or off when fail-safe mode is enabled. Upon power up, POR or UV_{SUP} event, the SWE timer starts, $t_{INACTIVE}$, which the processor has to configure theTCAN114x-Q1, clear the PWRON flag or configure the device for normal or listen mode before the SWE timer expires. This feature cannot be disabled for power up. If the device has not had the PWRON flag cleared or been placed into normal or listen mode, it enters sleep mode. The SWE timer can be disabled for the other scenarios that causes the device to enter fail-safe mode by setting SWE_DIS; 8'h1C[7] = 1 and FS_DIS at 8'h17[0] = 1.

The device wakes up for a CAN bus WUP or a local wake thus entering standby mode. Once in standby mode, the $t_{SILENCE}$ and $t_{INACTIVE}$ timers start. If $t_{INACTIVE}$ expires, the device re-enters sleep mode. When the device receives a CANINT, LWU or FRAME_OVF such that the device leaves sleep mode and enters standby mode, the processor has until $t_{INACTIVE}$ expires to clear the flags and place the device into normal mode. If this does not happen, the device enters sleep mode. When in standby, normal or listen mode and $t_{SILENCE}$ (SWE_DIS=1) or CANSLNT (SWE_DIS=0) persists for $t_{INACTIVE}$, the device enters sleep mode. Examples of events that could create this are the processor is no longer working and not able to exercise the SPI bus, a go to sleep command comes in and the processor is not able to receive it or is not able to respond.

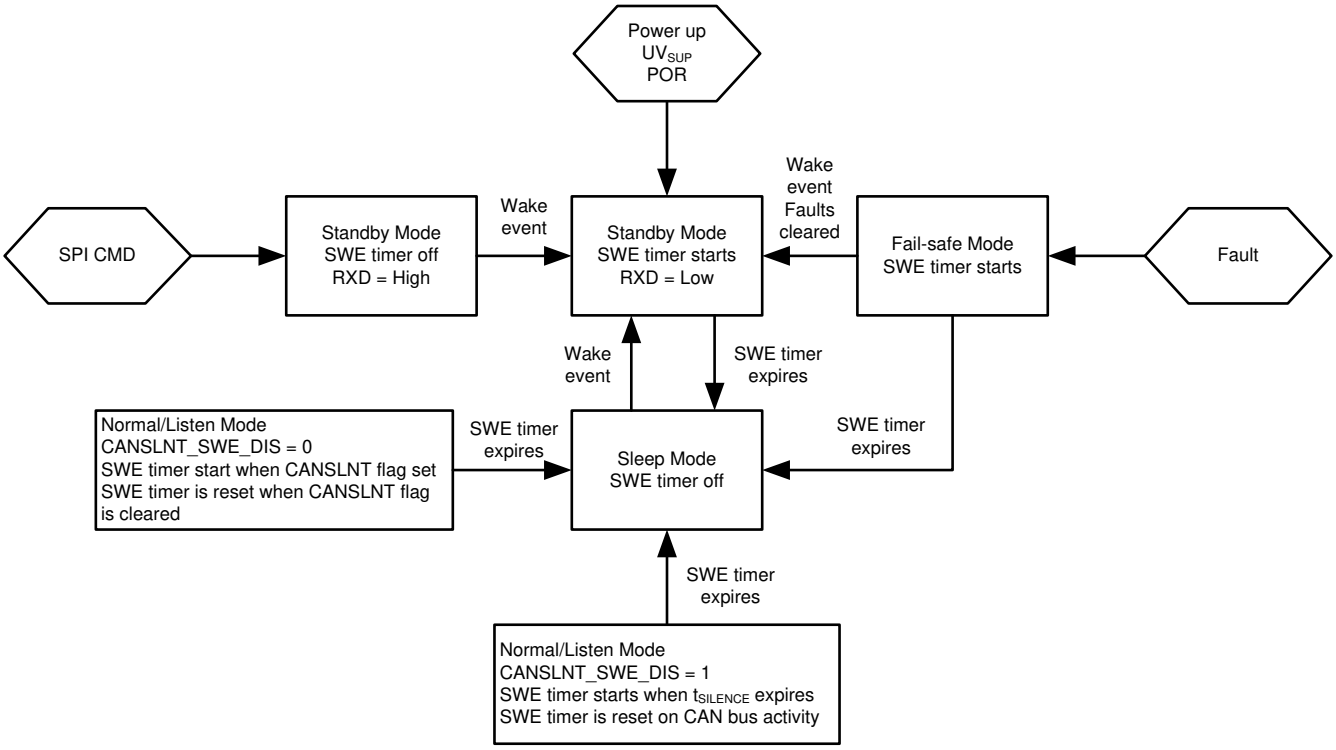


Figure 10-22. Sleep Wake Error (SWE) Timer

10.4.6.2 Fail-safe Mode

Fail-safe mode is a low power mode that different faults can cause the device to enter. Once in this mode, the SWE timer will start. This provides a window of time to clear the faults and receive a wake event. If the faults are not cleared or a wake event doesn't take place prior to $t_{INACTIVE}$ the device will enter sleep mode to reduce power consumption. The fault must be cleared before a wake event is recognized for the device to enter the correct operating mode. This mode is default on and can be disabled by setting register 8'h17[0] = 1. A fail-safe mode counter is available that after a set number of events in a row the device performs the programmed action which can include going to sleep and a WUP or LWU event does not wake the device. A power on reset is required. The counter is default disabled and can be enabled at 8'h17[7]. The counter expiration action is at 8'h17[6:4]. The number of events before action is programmed is set at 8'h18[7:4] with a value up to 15 events. 8'h18[3:0] is the running up/down fail-safe event counter that can be read and cleared.

If fail-safe mode is entered a global interrupt is issued, 8'h53[5] and the reason for entering fail-safe mode is provided by register 8'h17[3:1].

Note

- Fail-safe counter counts each event. The term "in a row" means each event that happens without the counter being cleared and does not mean within a specified time.
- The fail-safe counter should be cleared after each time the device enters fail-safe mode to avoid unwanted actions.

10.4.7 Protection Features

The TCAN114x-Q1 has several protection features that are described as follows.

10.4.7.1 Driver and Receiver Function

The TXD and RXD pins are input and output between the processor and the CAN physical layer transceiver. The digital logic input and output levels for these devices are TTL levels for compatibility with protocol controllers

having 1.8 V, 3.3 V or 5 V logic or I/O. Table 10-5 and Table 10-6 provides the states of the CAN driver and CAN receiver in each mode.

Table 10-5. Driver Function Table

DEVICE MODE	TXD INPUT	BUS OUTPUTS		DRIVEN BUS STATE
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Standby	X	Z	Z	Weak Pull to GND
Listen	X	Z	Z	Biased to ~ 2.5 V
Sleep	X	Z	Z	Weak Pull to GND

Table 10-6. Receiver Function Table Normal and Standby Modes

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD TERMINAL
Normal/Listen	$V_{ID} \geq 0.9$ V	Dominant	L
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	H
Standby/Sleep	$V_{ID} \geq 1.15$ V	Dominant	See Figure 10-12
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	H

10.4.7.2 Floating Terminals

There are internal pull ups on critical terminals to place the device into known states if the terminal floats. See Table 10-7 for details on terminal bias conditions.

Table 10-7. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
SCLK	Pull up	Weakly biases input
SDI	Pull up	Weakly biases input
nCS	Pull up	Weakly biases input so the device is not selected
RXD	Pull up	Active when CAN transceiver is off.
TXD	Pull up	Weakly biases input

Note

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a fail-safe protection. Special care needs to be taken when the device is used with MCUs using open drain outputs.

10.4.7.3 TXD Dominant Time Out (DTO)

The TCAN114x-Q1 supports dominant state time out. This is an internal function based upon the TXD path. The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant (LOW) longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen on TXD terminal, thus clearing the time out constant of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal (HIGH) is seen on TXD terminal; thus, clearing the dominant time out. The receiver remains active and the RXD terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD DTO fault. This feature can be disabled by using register 8'h10[6] = 1b, DTO_DIS.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame.

10.4.7.4 CAN Bus Short Circuit Current Limiting

These devices have several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state for a system fault. During CAN communication the bus switches between dominant and recessive states; thus, the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Receive \times IOS(SS)\_REC] \quad (1)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

Note

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate V_{SUP}.

10.4.7.5 Thermal Shutdown

The TCAN114x-Q1 has two trigger points for thermal events. The first is a thermal shutdown warning. Once the temperature exceeds this limit, an interrupt is issued. The second is the actual thermal shutdown (TSD) event. This is a device preservation event. If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN transceiver and CAN transceiver circuitry, thus blocking the signal to bus transmission path. A thermal shut down interrupt flag is set, and an interrupt is inserted so that the microprocessor is informed. If this event happens, other interrupt flags may be set as an example a bus fault where the CAN bus is shorted to V_{BAT}. When this happens, the digital core and SPI interface is still active. After a time of ≈ 300 ms the device checks the temperature of the junction. Thermal shutdown timer, t_{TSD}, starts when TSD fault event starts and exit to sleep mode when TSD fault is not present when TSD timer is expired. While in thermal shut down protected mode, a SPI write to change the device to either Normal or Standby mode is ignored while writes to change to sleep mode are accepted.

If the TSD event takes place and fail-safe mode is enabled, the same process takes place with and instead off thermal shut down protected stated it enters fail-safe mode.

Note

If a thermal shut down event happens while the device is experiencing a V_{IO} under voltage event, the device enters sleep mode if fail-safe mode is disabled.

10.4.7.6 Under-Voltage Lockout (UVLO) and Unpowered Device

There are three under voltage events monitored in the TCAN114x-Q1, V_{SUP}, V_{IO} and V_{CC}. The three supply terminals are input sources for the TCAN114x-Q1 and have under voltage detection circuitry which places the device in a protected state if an under-voltage fault occurs, UV_{SUP}, UV_{CC} and UV_{IO}. This protects the bus during in under voltage event on these terminals. If V_{SUP} is under voltage the device loses the source needed to keep the internal regulators active. This causes the device to go into a state where communication between the microprocessor and the TCAN114x-Q1 is disabled. The TCAN114x-Q1 is not able to receive information from the bus; and thus, does not pass any signals from the bus, including any Bus Wake via BWRR signals to the microprocessor. See Table 10-9. For under voltage events, there is a filter time, t_{UVFLTR}, that the even must last longer than for the t_{UVSLP} timer to start. Once the t_{UVSLP} timer expires and the under-voltage condition is still present, the device enters sleep mode or fail-safe mode if enabled.

10.4.7.6.1 UV_{SUP}, UV_{CC}

If UV_{SUP} decreases to trip point, the device is in standby mode. A UV_{SUP} event causes the INH pin to turn off. When the V_{SUP} is greater than UV_{SUP} and INH turns on the SWE timer will start. If V_{SUP} decreases more, the TCAN114x-Q1 shuts everything down as the POR level has been reach and when V_{SUP} returns, the device comes up as if it is the initial power on. All registers are cleared and the device has to be reconfigured. If an under-voltage event takes place on the V_{CC} pin, the device starts t_{UVSLP} timer to determine if this is a real event. If after the timer times out, the device enters fail-safe or sleep mode depending upon device set up. See Figure 10-23. The TCAN114x-Q1 also provides voltage over protection on the V_{CC} input. Once detected, the device enters fail-safe or sleep mode depending upon device set up. See Table 10-8 for the relationship between V_{SUP} and V_{CC}.

Table 10-8. UV_{SUP}, UV_{CC}

V_{SUP}	V_{CC}	DEVICE STATE	BUS	RXD
> UV_{SUP}	> UV_{CC}	Normal	Per TXD	Mirrors Bus
> UV_{SUP}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High (Recessive)
< UV_{SUP}	NA	Power off	High Impedance	High Impedance

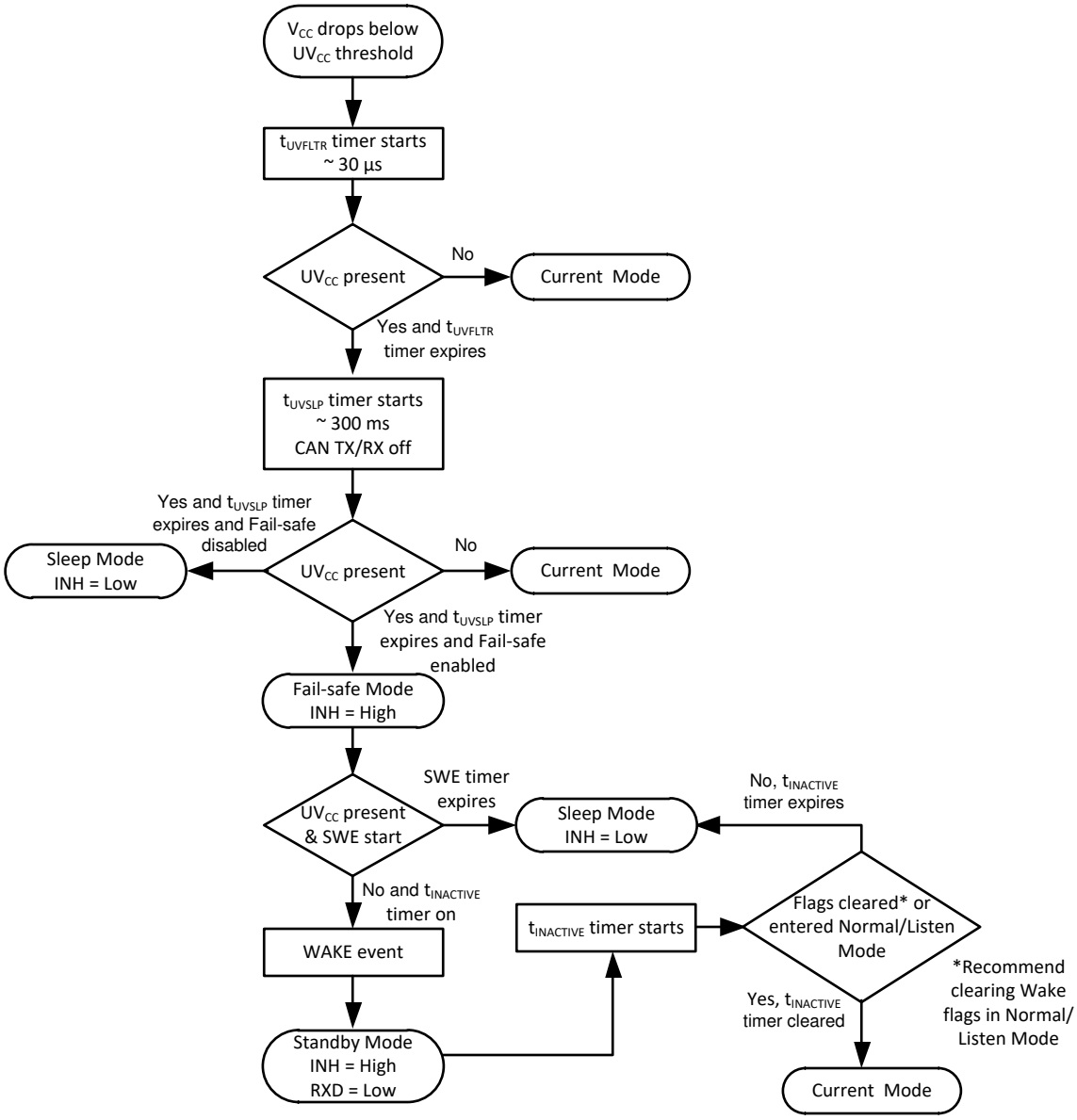


Figure 10-23. UV_{CC} State Diagram

10.4.7.6.2 UV_{IO}

If V_{IO} drops below UV_{IO} under-voltage detection several functions are disabled. The transceiver switches off and disengages from the bus until V_{IO} has recovered. When UV_{IO} triggers, the t_{UV} timer starts. If the timer times out and the UV_{IO} is still there, the device enters sleep mode. See Figure 10-8, Figure 10-9. Once in sleep mode, a wake event is required to place the TCAN114x-Q1 into standby mode and enable the INH pin. As registers are cleared in sleep mode, the UV_{IO} interrupt flag is lost. If the UV_{IO} event is still in place, the cycle repeats. If during a thermal shut down event a UV_{IO} event happens, the device automatically enters sleep mode. See Figure 10-24 on how UV_{IO} behaves.

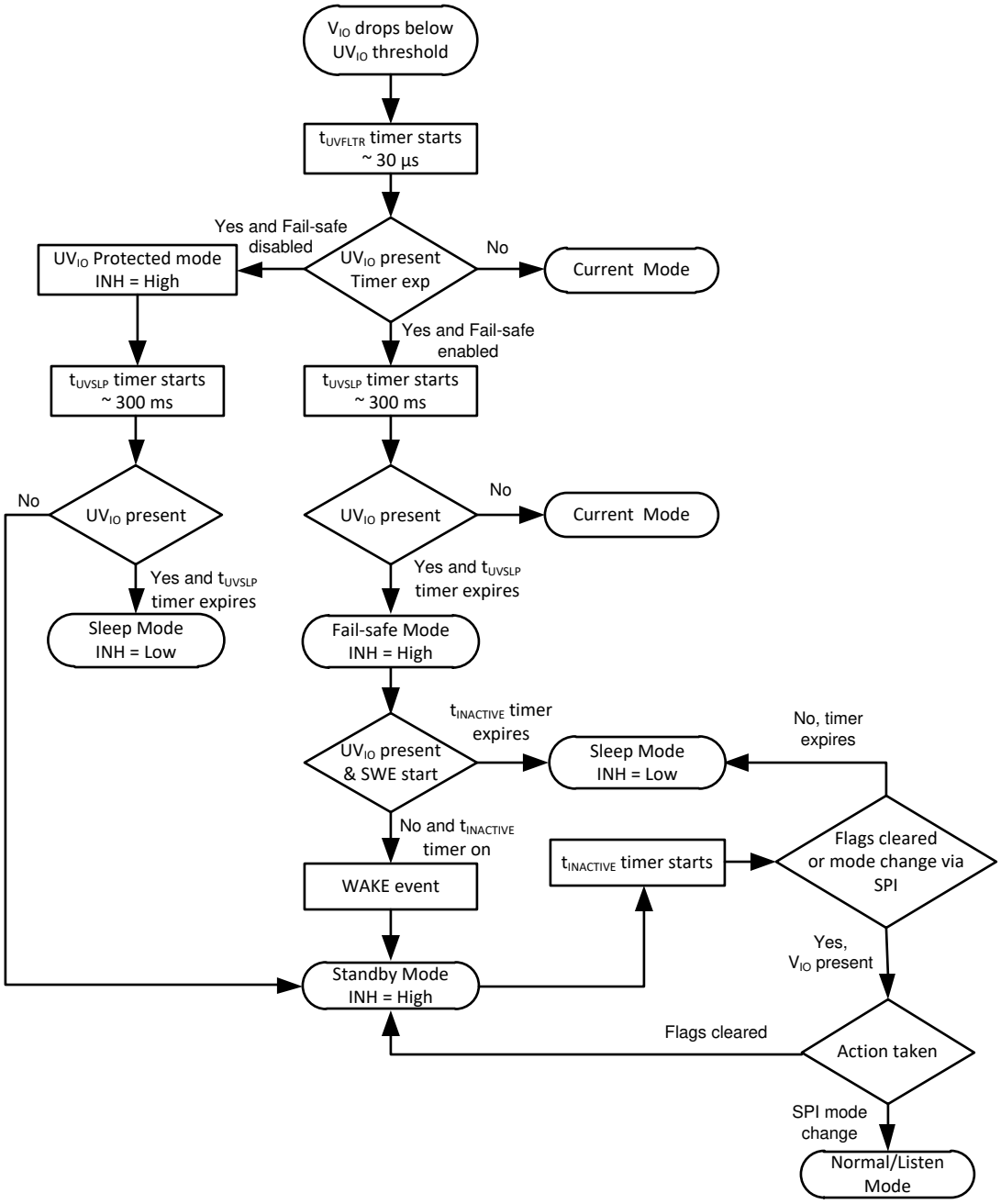


Figure 10-24. UV_{IO} State Diagram

The device is designed to be an "ideal passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have extremely low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

10.4.7.6.2.1 Fault Behavior

During a UV_{IO}, UV_{CC} or TSD fault the TCAN114x-Q1 automatically does the following to keep the digital core in a known state.

Table 10-9. Under Voltage Lockout I and O Level Shifting Devices

V_{SUP}	V_{IO}	V_{CC}	DEVICE STATE	BUS	RXD
> UV_{SUP}	> UV_{IO}	> UV_{CC}	Normal	Per TXD	Mirrors Bus
> UV_{SUP}	> UV_{IO}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High (Recessive)
< UV_{SUP}	> UV_{IO}	NA	Power Off	High Impedance	High (Recessive)
> UV_{SUP}	< UV_{IO}	> UV_{CC}	Fail-safe or UV_{IO} Protected → Sleep	High Impedance	High Impedance
> UV_{SUP}	< UV_{IO}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High Impedance
< UV_{SUP}	< UV_{IO}	NA	Power Off	High Impedance	High Impedance

Note

Once an under-voltage condition and interrupt flags are cleared and the V_{SUP} supply has returned to valid level the device typically needs t_{MODE_x} to transition to normal operation. The host processor should not attempt to send or receive messages until this transition time has expired. If V_{SUP} has an under-voltage event, the device goes into a protected mode which disables the wake-up receiver and places the RXD output into a high impedance state.

10.4.7.7 Watchdog (TCAN1144-Q1 and TCAN1146-Q1)

The TCAN114x-Q1 has an integrated watchdog function. The TCAN114x-Q1 provides a window-based watchdog as well as a selectable time-out and question and answer (Q&A) watchdog using SPI programming. This function is default disabled. When enabled, the watchdog timer does not start until the first input trigger event when in normal and standby (when enabled) operational modes. The watchdog timer is off in sleep mode. The INH pin can be programmed as a LIMP function which provides a limp home capability when connected to external circuitry. Otherwise the nINT will reflect a watchdog failure and any specific programmed action. When in sleep mode, the limp pin is off. When the error counter reaches the watchdog trigger event level, the limp pin turns on connecting V_{SUP} to the pin as described in the LIMP pin section.

10.4.7.7.1 Watchdog Error Counter

The TCAN114x-Q1 has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter is set to trigger a watchdog error event. This counter can be change to the fifth or ninth error. The error counter can be read at register 8'h13[3:2].

10.4.7.7.2 Watchdog SPI Control Programming

The watchdog is configured and controlled using registers 8’h13 through 8’h15. These registers are provided in table Table 10-10. The TCAN114x-Q1 watchdog can be set as a time-out, window or question and answer (Q&A) watchdog by setting 8’h13[7:6] to the method of choice. The time-out and window watchdog timer is based upon registers 8’h13[5:4] WD prescaler and 8’h14[7:5] WD timer and is in ms. See Table Table 10-10 for the achievable times. If using smaller time windows, it is suggested to use the Time-out version of the watchdog. This is for times between 4 ms and 64 ms.

Table 10-10. Watchdog Window and Time-out Timer Configuration (ms)

WD_TIMER (ms)	8'h13[5:4] WD_PRE			
8'h14[7:5]	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192

Table 10-10. Watchdog Window and Time-out Timer Configuration (ms) (continued)

WD_TIMER (ms)	8'h13[5:4] WD_PRE			
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

Note

If timing parameters are changed while the watchdog is running, the WD stops until after the first input trigger event after the new parameters have been programmed at which time it runs based upon the new timing parameters.

10.4.7.7.3 Watchdog Timing

The TCAN114x-Q1 provides three methods for setting up the watchdog. If more frequent, < 64 ms, input trigger events are desired it is suggested to us the Time-out timer as this is an event within the time event and not specific to an open window.

When using the window watchdog, it is important to understand the closed and open window aspects. The TCAN114x-Q1 is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be considered. Using the 60 ms nominal total window provides a closed and open window that are each 30 ms. Taking the ± 10% internal oscillator into account means the total window could be 54 ms, t_{WINDOW}, MIN or 66 ms, t_{WINDOW} MAX. The closed and open window would then be 27 ms, T_{WDOUT} MIN, or 33 ms, T_{WDOUT} MIN. From the 54 ms total window and 33 ms closed window the total open window is 21 ms. The trigger event needs to happen at the 43.5 ms ± 10.5 ms, safe trigger area. The same method is used for the other window values. Figure 10-25 provides the above information graphically. Once the WD trigger is written, the current Window is terminated and a new Closed Window is started.

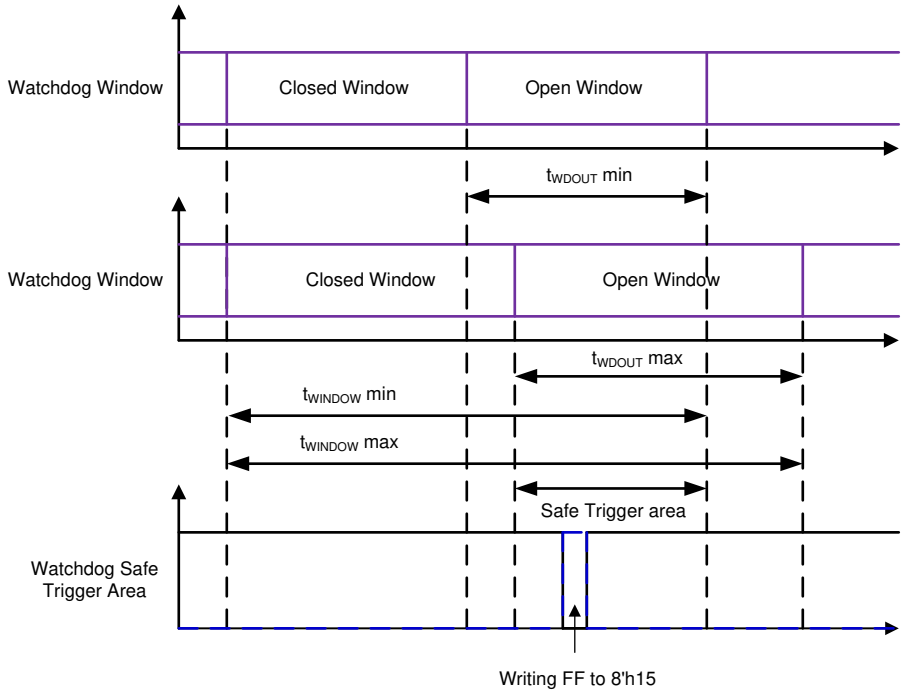


Figure 10-25. Window Watchdog Timing Diagram

10.4.7.7.4 Question and Answer Watchdog

The TCAN114x has a watchdog timer that supports the window watchdog as well as the Q&A watchdog.

Section 10.4.7.7.5 explains the WD initialization events.

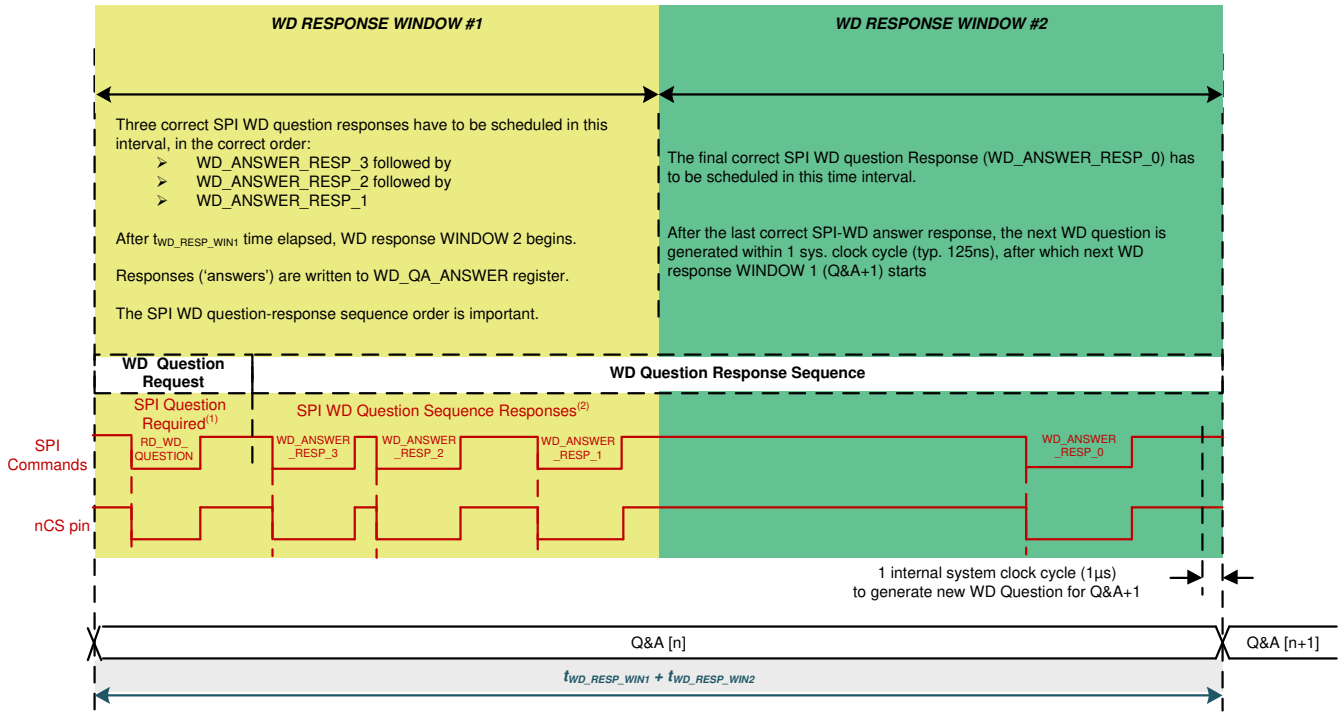
10.4.7.7.4.1 WD Question and Answer Basic information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdog via a SPI write or a pin toggle, the MCU reads a 'question' from the TCAN114x, do math based on the question and then write the computed answers back to the TCAN114x. The correct answer is a four byte response. Each byte must be written in order and with the correct timing to have a correct answer.

There are two watchdog windows; referred to as WD Response window #1 and WD Response window #2 (Figure 10-26 WD QA Windows as example). The size of each window will be 50% of the total watchdog time, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is the MCU reads the question, when the question is read, the timer starts. The CPU must perform a mathematical function on the question, resulting in four bytes of answers. Three of the four answer bytes must be written to the answer register within the first window, in correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all four answer bytes were correct and in the correct order, then the response is considered good and a new question is generated, starting the cycle over again. Once the fourth answer is written into WD Response Window #2, that window is terminated and a new WD Response Window #1 is started.

If anything is incorrect or missed, the response is considered bad and the watchdog question will NOT change. In addition, an error counter will be incremented. Once this error counter hits a threshold (defined in the WD_ERR_CNT register field), the watchdog failure action will be performed. Examples of actions are an interrupt, or reset toggle, etc.



A. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.

B. The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 10-26. WD Q&A Sequence Run for WD Q&A Multi-Answer Mode

10.4.7.7.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, Table 10-11.

Table 10-11. List of Watchdog Related Registers

Register Address	Register Name	Description
0x13	WD_CONFIG_1	Watchdog configuration and action in event of a failure
0x14	WD_CONFIG_2	Sets the time of the window, and shows current error counter value
0x15	WD_INPUT_TRIG	Register to reset or start the watchdog
0x16	WD_RST_PULSE	Reset pulse width in event of watchdog failure
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers mainly deal with setting up the watchdog window time length. Refer to Table 10-10 to see the options for window sizes, and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, it is recommended that windows greater than 64 ms be used when using the QA watchdog functionality.

There are also different actions that can be performed when the watchdog error counter hits the error counter threshold.

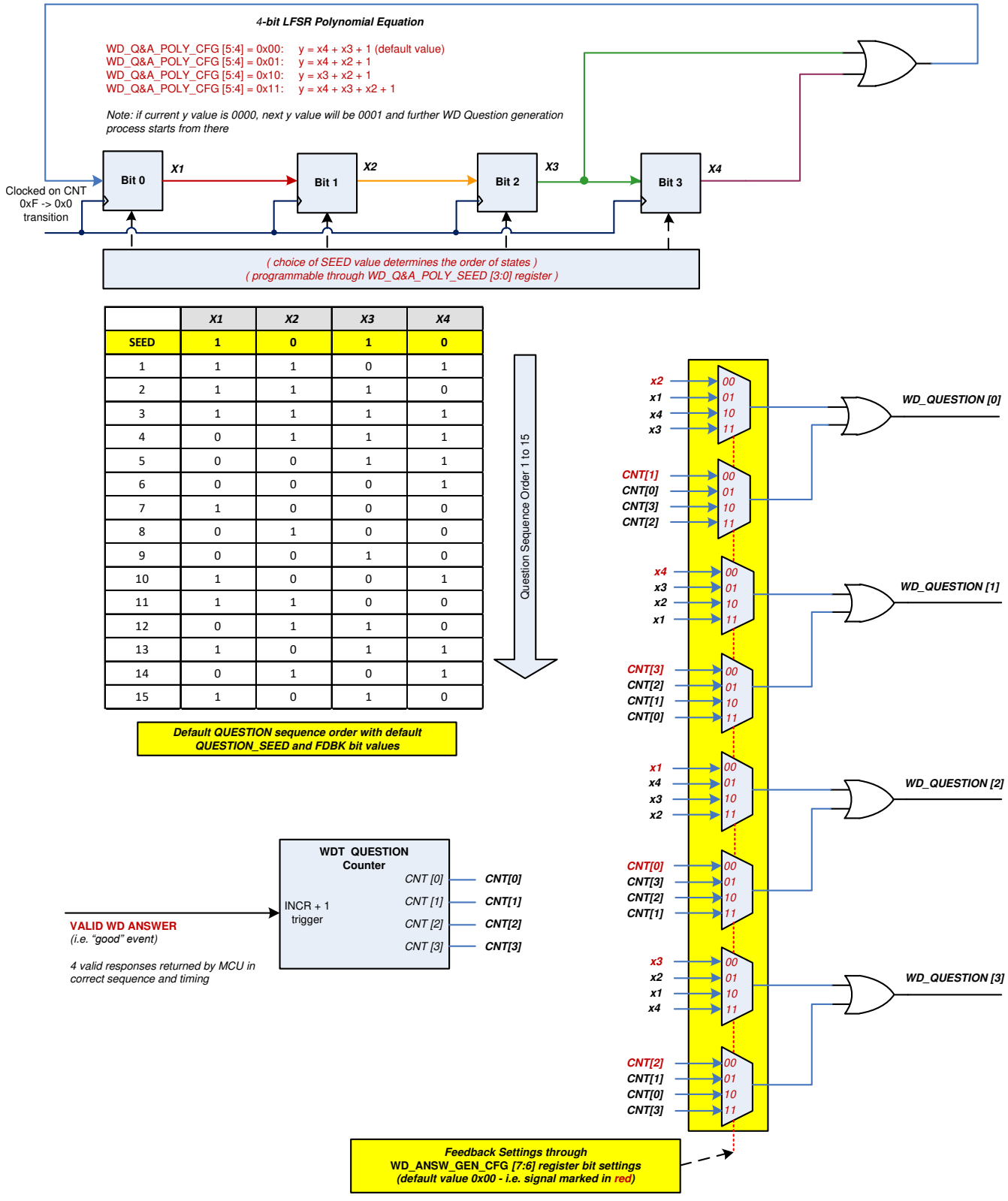
10.4.7.7.4.3 WD Question and Answer Value Generation

The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- For WD Q&A multi-answer:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.

The WD question value is latched in the WD_QUESTION[3:0] bits of the WD_QA_QUESTION register and can be read out at any time.

The Markov chain process is clocked by the 4-bit Question counter at the transition from b1111 to b0000. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QUESTION [3:0] generation is given in Figure 10-27.



	X1	X2	X3	X4
SEED	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

A. If the current *y* value is 0000, the next *y* value is 0001. The next watchdog question generation process starts from that value.

Figure 10-27. Watchdog Question Generation

Table 10-12 contains the answers for each question, as long as the question polynomial and answer generation configuration are both at their default values.

Table 10-12. Example answers to questions with default settings

QUESTION IN WD_QUESTION_VALUE REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT 2'b11	WD_ANSW_CNT 2'b10	WD_ANSW_CNT 2'b01	WD_ANSW_CNT 2'b00
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

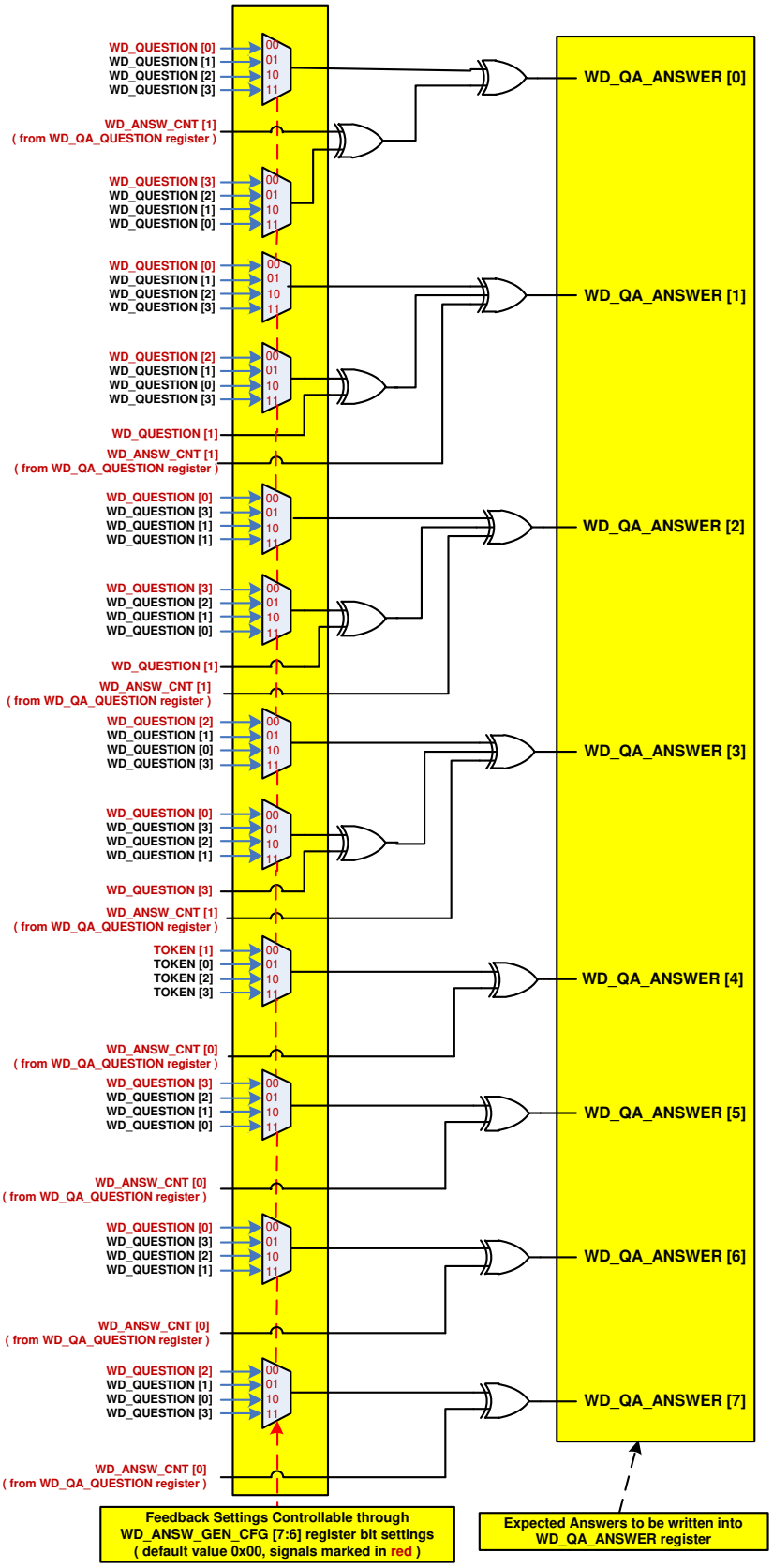


Figure 10-28. WD Expected Answer Generation

Table 10-13. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (WD_CFG = 0b)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WD_QA_QUESTION REGISTER		COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		QA_ANSW_ERR	WD_ERR(1)	
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	No answers
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Total WD_ANSW_CNT[1:0] = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer				
2 CORRECT answer	1 CORRECT answer				
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer				
2 CORRECT answer	1 INCORRECT answer				
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answer				
2 CORRECT answer	2 CORRECT answer				
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answer				
2 CORRECT answer	2 INCORRECT answer				
0 answer	3 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	
2 INCORRECT answer	1 CORRECT answer				
0 answer	3 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answer				
2 INCORRECT answer	1 INCORRECT answer				
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answer		1b	1b	
2 INCORRECT answer	2 CORRECT answer				
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answer				
2 INCORRECT answer	2 INCORRECT answer				
3 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	0b	1b	Less than 4 CORRECT ANSW in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answer	0 answer		0b	1b	
1 CORRECT answer	0 answer				
3 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	0b	CORRECT SEQUENCE

Table 10-13. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (WD_CFG = 0b) (continued)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WD_QA_QUESTION REGISTER		COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		QA_ANSW_ERR	WD_ERR(1)	
3 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] < 4
3 INCORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
4 CORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	
3 CORRECT answer + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
2 CORRECT answer + 2 INCORRECT answer	Not applicable				
1 CORRECT answer + 3 INCORRECT answer	Not applicable				

(1) WD_ERR is the logical OR of all WD errors.

10.4.7.7.5 Question and Answer WD Example

For this example, we'll walk through a single sequence with the following configuration settings, Table 10-14.

Table 10-14. Example Configuration Settings

Item	Value	Description
Watchdog window size	1024 ms	Window size of 1024 ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	9 (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

10.4.7.7.5.1 Example configuration for desired behavior

Table 10-15 register writes will configure the part for the example behavior specified above. Most of the settings are power on defaults.

Table 10-15. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11011101 / 0xDD
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_RST_PULSE (0x16)	[W] 0b00001110 / 0x0E
4	WD_QA_CONFIG (0x2D)	[W] 0b00001010 / 0x0A

10.4.7.7.5.2 Example of performing a question and answer sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the four answer bytes
3. Send three of them within the first response window
4. Wait and send the last byte in the second response window

See Table 10-16 for an example of the first loop sequence.

Table 10-16. Example First Loop

Step	Register	Data	Description
1	WD_INPUT_TRIG (0x15)	[W] 0xFF	Start the watchdog (since it isn't started yet), also keep a timer internally to flag when response window 1 ends and window 2 starts.
2	WD_QA_QUESTION (0x2F)	[R] 0x3C	Read the question. Question is 0x3C
3	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3 (See Table 10-12 Example answers to questions with default settings to see answers)
4	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
5	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
6	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

At this point, you can read the WD_QA_QUESTION (0x2F) register to see if the error counter has increased or if QA ERROR is set.

10.4.8 Bus Fault Detection and Communication (TCAN1144-Q1 and TCAN1146-Q1)

The TCAN1144-Q1 and TCAN1146-Q1 provide advanced bus fault detection. TCAN1146-Q1 is used for illustration purposes. The device can determine certain fault conditions and set a status/interrupt flag so that the MCU can understand what the fault is. Detection takes place and is recorded if the fault is present during

four dominant to recessive transitions with each dominant bit being ≥ 2 µs. As with any bus architecture where termination resistors are at each end not every fault can be specified to the lowest level, meaning exact location. The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there is a short to battery, short to ground, short to each other or opens. From a system perspective, the location of the device can impact what fault can be detected. See Figure 10-29 as an example of node locations and how they can impact the ability to determine the actual fault location. Figure 10-30 through Figure 10-34 show the various bus faults based upon the three-node configuration. Table 10-17 shows what can be detected and by which device. Fault 1 is detected as ½ termination and Fault 2 is detected as no termination.

Bus fault detection is a system-level situation. If the fault is occurring at the ECU then the general communication of the bus is compromised. For complete coverage of a node a system level diagnostic step for each node and the ability to communicate this back to a central point is needed.

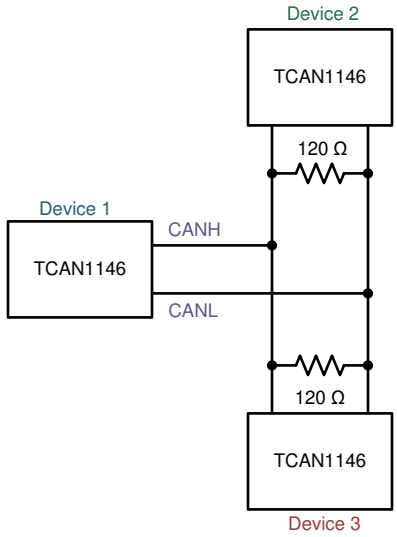
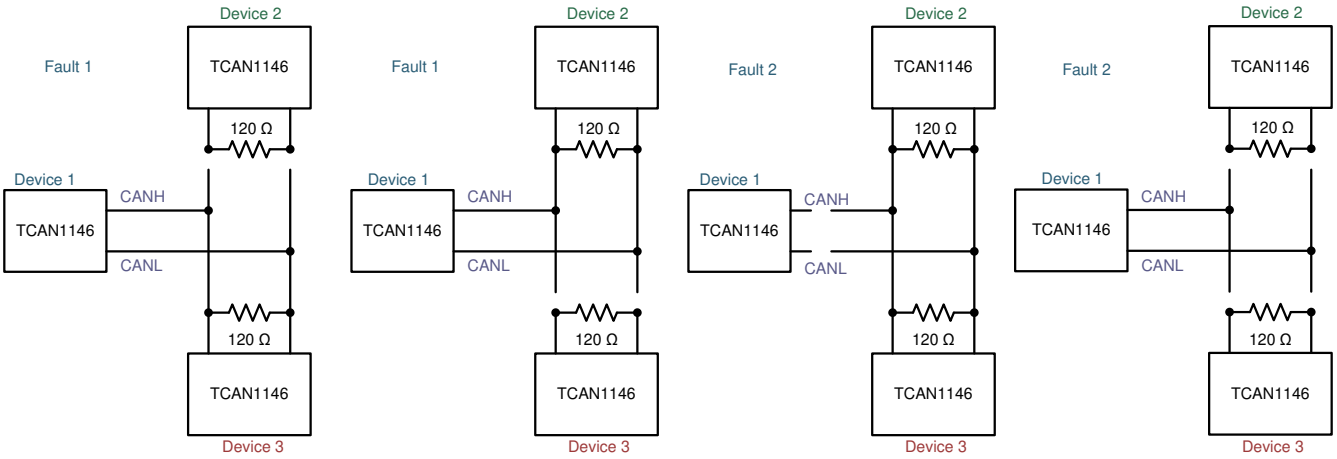


Figure 10-29. Three-Node Example



- Fault 1 is any case where ½ termination is seen
- Fault 2 is any case where no termination is seen

Figure 10-30. Open Fault 1 and 2 Examples

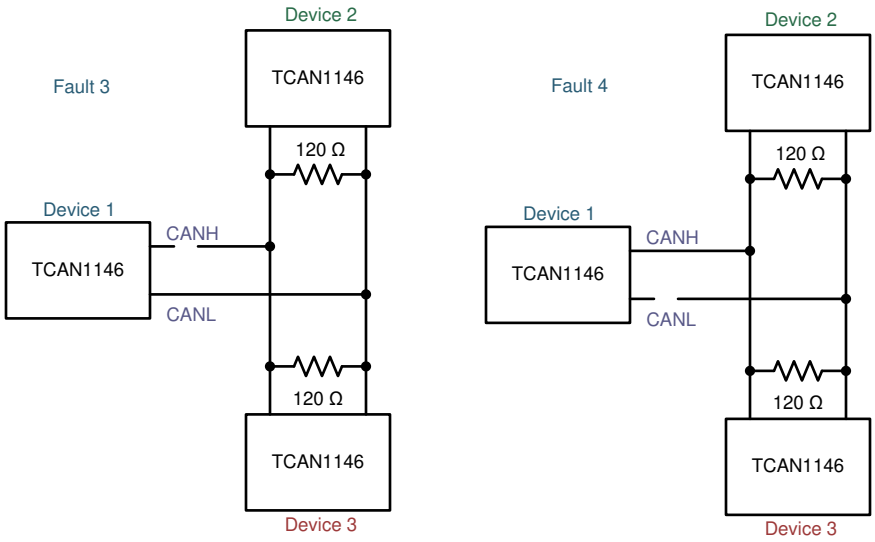


Figure 10-31. Open Fault 3 and 4 Examples

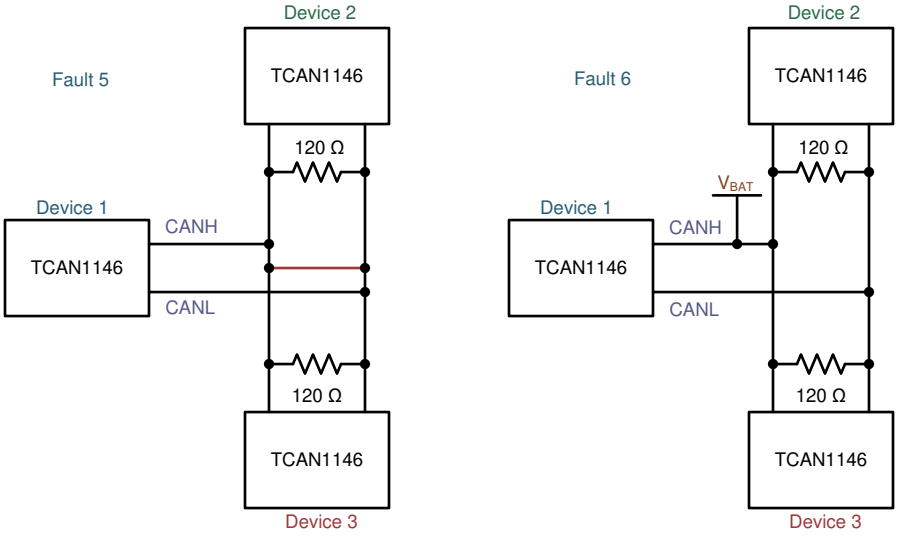


Figure 10-32. Fault 5 and 6 Examples

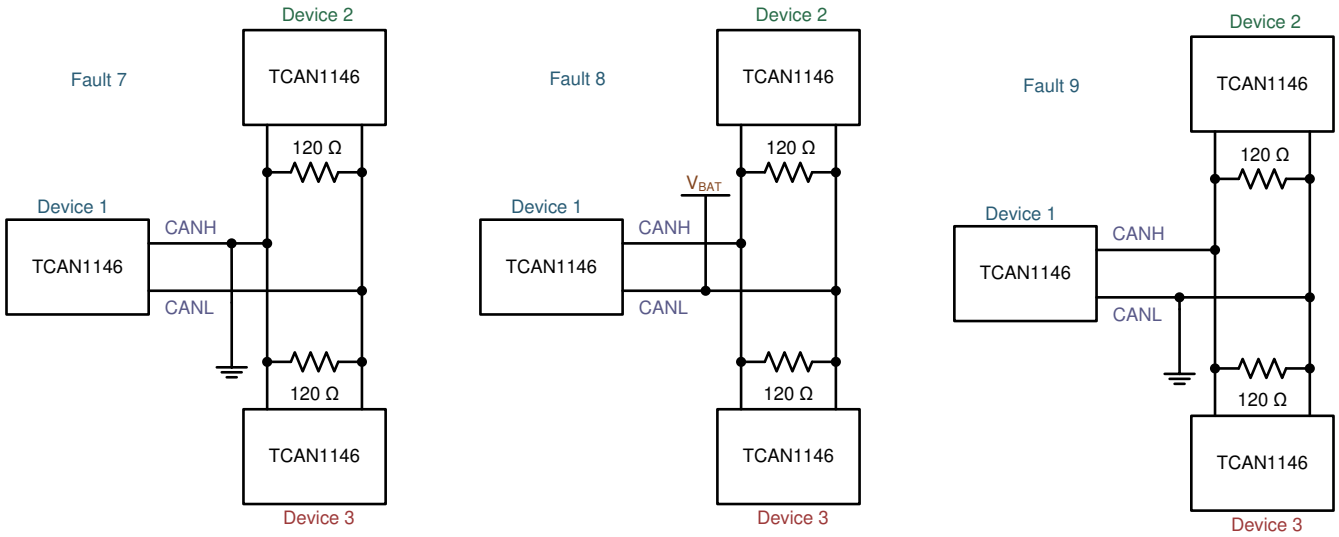


Figure 10-33. Fault 7, 8 and 9 Examples

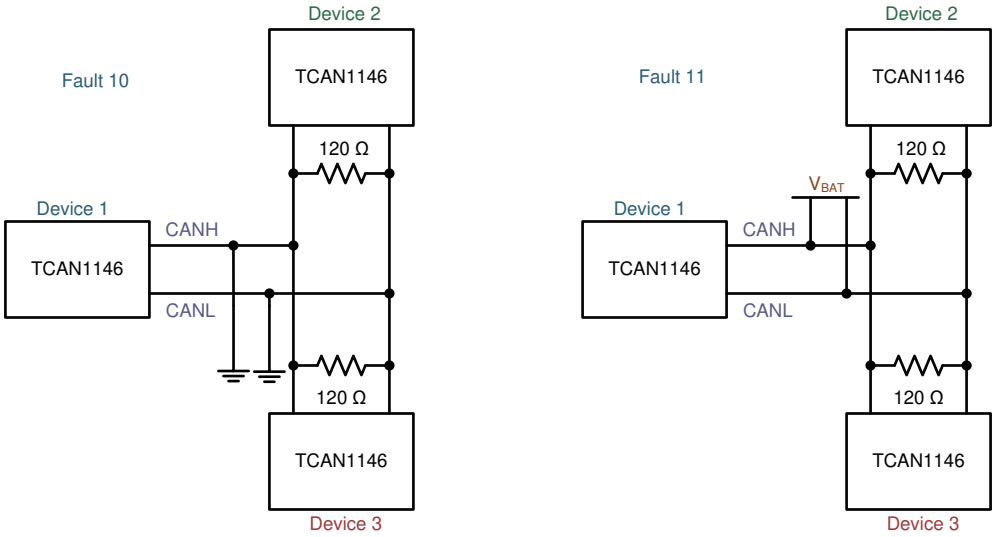


Figure 10-34. Fault 10 and 11 Examples

Table 10-17. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Fault Detected
1	Open	Open	All positions see this fault as half termination and detect them
2	Open	Open	Depending upon open location the device detects this as no termination.
3	Open	Normal	Yes, but cannot tell the difference between it and Fault 2 and 4; Device 2 and Device 3 does not see this fault
4	Normal	Open	Yes, but cannot tell the difference between it and Fault 2 and 3; Device 2 and Device 3 does not see this fault
5	Shorted to CANL	Shorted to CANH	Yes, but not location
6	Shorted to V_{bat}	Normal	Yes, but not location
7	Shorted to GND	Normal	Yes, but cannot tell the difference between this and Fault 10
8	Normal	Shorted to V_{BAT}	Yes, but cannot tell the difference between this and Fault 11
9	Normal	Shorted to GND	Yes, but not location
10	Shorted to GND	Shorted to GND	Yes, but cannot tell the difference between this and Fault 7
11	Shorted to V_{bat}	Shorted to V_{BAT}	Yes, but cannot tell the difference between this and Fault 8

Table 10-18. Bus Fault Interrupt Flags Mapping to Fault Detection Number

Address	BIT(S)	DEFAULT	FLAG	DESCRIPTION	FAULT DETECTED	ACCESS
8'h54	7	1'b0	RSVD	Reserved		
	6	1'b0	CANBUSTERMOPEN	CAN Bus has one termination point open	Fault 1	R/WC
	5	1'b0	CANHCANL	CANH and CANL Shorted Together	Fault 5	R/WC
	4	1'b0	CANHBAT	CANH Shorted to V_{BAT}	Fault 6	R/WC
	3	1'b0	CANLGND	CANL Shorted to GND	Fault 9	R/WC
	2	1'b0	CANBUSOPEN	CAN Bus Open (One of three possible places)	Faults 2, 3 and 4	R/WC
	1	1'b0	CANBUSGND	CANH Shorted to GND or Both CANH & CANL Shorted to GND	Faults 7 and 10	R/WC
	0	1'b0	CANBUSBAT	CANL Shorted to V_{BAT} or Both CANH & CANL Shorted to V_{BAT}	Faults 8 and 11	R/WC

10.4.9 SPI Communication

The Serial Peripheral Interface (SPI) uses a standard configuration. Physically the digital interface pins are nCS (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out) and SCLK (Serial Clock). Each SPI transaction is a 16, 24 or 32 bits containing an address and read/write command bit followed by one to three data bytes. Supporting two and three data bytes is accomplished utilizing burst read and write where the address is automatically incremented for the data along with the same number of clock cycles per bit. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (byte).

The SPI data input data on SDI is sampled on the low to high edge of the clock (SCLK). The SPI output data on SDO is changed on the high to low edge of the clock (SCLK).

When programming the device in sleep mode, care must be taken to understand what the output is. An example is the device is programmed with fail-safe mode off and one of the fault conditions that puts the device in sleep mode takes place, like an UV_{CC}. While in sleep mode, fail-safe mode is enabled. the device stays in sleep mode and does not switch to fail-safe mode.

10.4.9.1 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the Serial Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

10.4.9.2 SPI Clock Input (SCLK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of SCLK and the SPI Data Output is changed on the falling edge of the SCLK. See Figure 10-35.

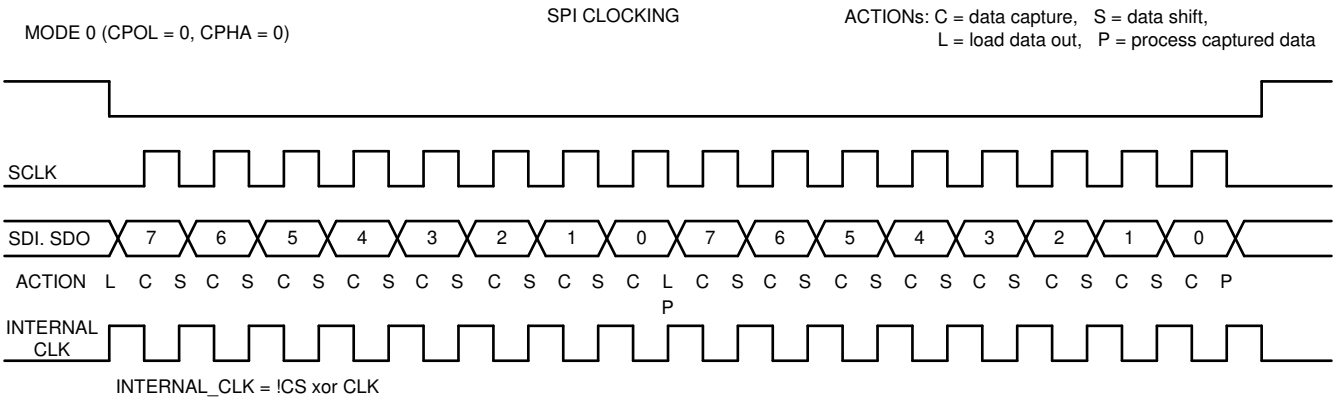


Figure 10-35. SPI Clocking

10.4.9.3 SPI Serial Data Input (SDI):

The SDI pin is used to let the device know which address is being read from or written to. During a write, the number of clock cycles determines how many data bytes up to three will be loaded into sequential addresses. The minimum number of clock cycles for a write is 16 supporting the initial address and write command followed by one byte of data as seen in Figure 10-36. The TCAN114x-Q1 supports burst read and write. Figure 10-37 shows an example of a 32-bit write which includes the initial 7-bit address, write bit and three data bytes. This all requires 32 clock cycles. Once the SPI is enabled by a low on nCS, the SDI samples the input data on each rising edge of the SPI clock (SCLK). The data is shifted into an appropriately-sized shift register and after the correct number of clock cycles the shift register is full and the SPI transaction is complete. For a write command code, the new data is written into the addressed register only after the exact number of clock cycles have been shifted in by SCLK and the nCS has a rising edge to deselect the device. For a burst write if there are 31 clock cycles of SCLK (1 clock cycle less than the full 3 byte write), the third byte write won't happen while the first two bytes write will be executed. If the correct number of clock cycles and data are not shifted in during one SPI transaction (nCS low), the SPIERR flag is set.

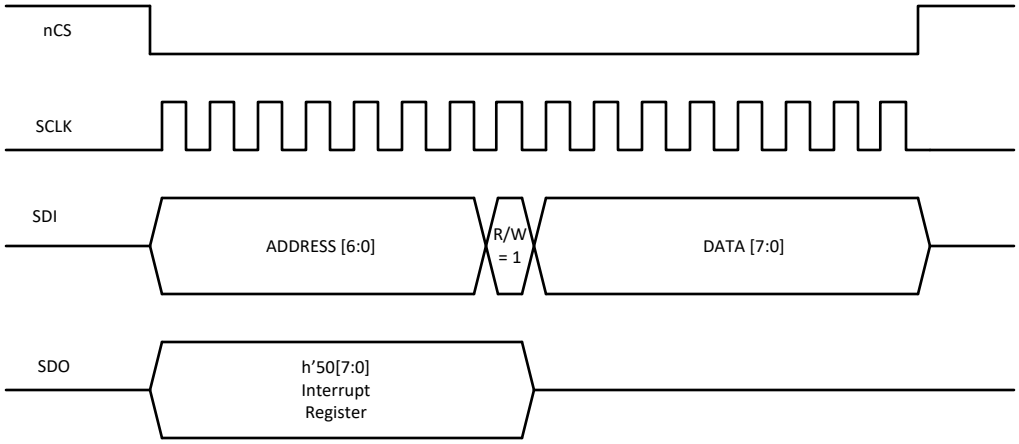


Figure 10-36. SPI Write

Example on how to write three bytes of data from one SPI write command.

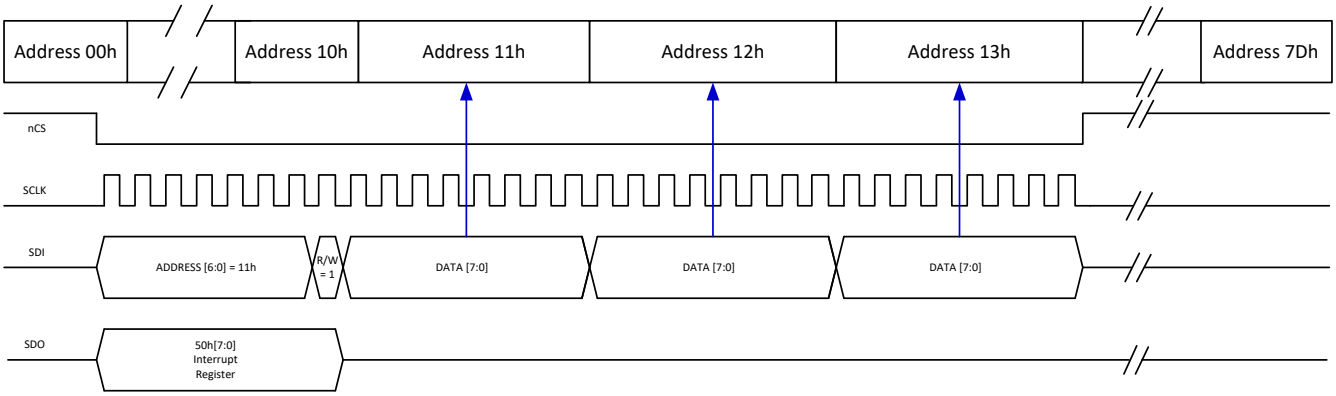


Figure 10-37. 32-bit SPI Burst Write

10.4.9.4 SPI Serial Data Output (SDO):

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the global interrupt register 8'h50, bit 7. The Global Interrupt register, INT_GLOBAL, is the first byte to be shifted out. The SDO pin provides data out from the device to the processor. For a write command this is the only data that will be provided on the SDO pin. For a read command the one to three bytes of data from successive address will be provided on the SDO line. Figure 10-38 and Figure 10-39 shows examples of a single address read and of a three sequential address read utilizing the 32-bit burst read. The 32-bit burst read shows the global interrupt register followed by the three requested data bytes.

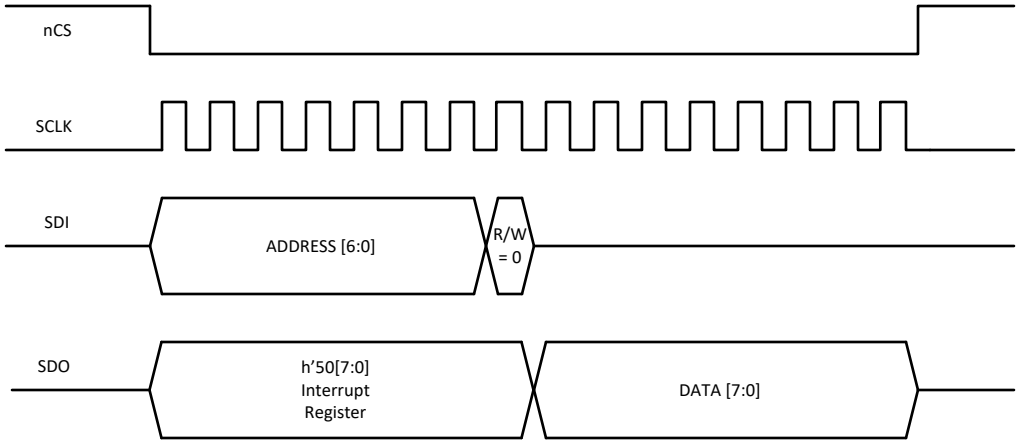


Figure 10-38. SPI Read

Example on how to read three bytes of data from one SPI read command.

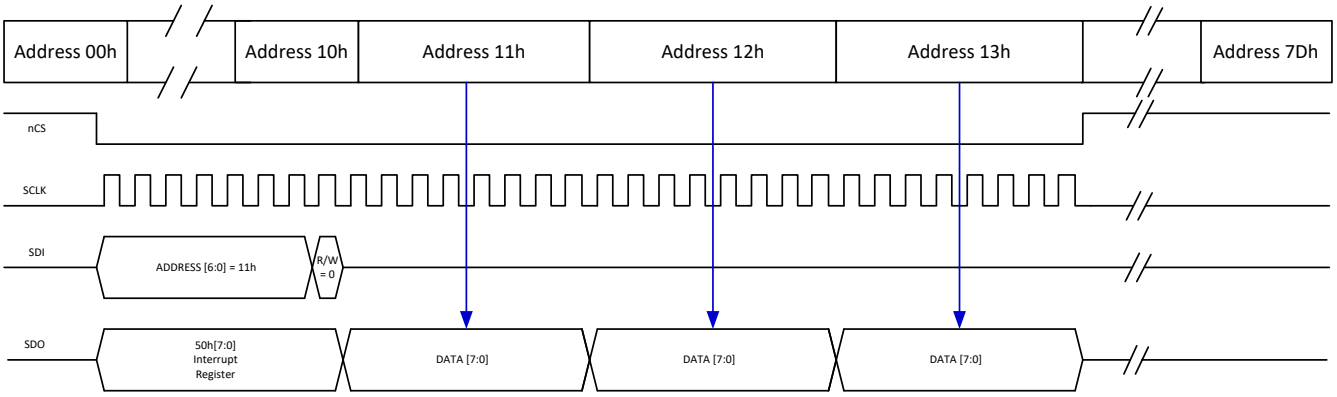


Figure 10-39. 32-bit SPI Burst Read

Note

If a read happens faster than 2 µs after a write the global fault flag status may not reflect any status change that the write may have initiated.

10.5 Programming

The TCAN114x-Q1 uses 7-bit addressing with a read/write bit followed by one to three bytes of data.

10.6 Register Maps

The TCAN114x-Q1 has a comprehensive register set with 7-bit addressing.

Table 10-19 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 10-19 should be considered as reserved locations and the register contents should not be modified.

Table 10-19. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Section 10.6.1
8h	REV_ID_MAJOR	Major Revision	Section 10.6.2
9h	REV_ID_MINOR	Minor Revision	Section 10.6.3
Ah + formula	SPI_RSVD_x	SPI reserved registers	Section 10.6.4
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Section 10.6.5
10h	MODE_CNTRL	Mode configurations	Section 10.6.6
11h	WAKE_PIN_CONFIG	WAKE pin configuration	Section 10.6.7
12h	PIN_CONFIG	Pin configuration	Section 10.6.8
13h	WD_CONFIG_1(1)	Watchdog configuration 1	Section 10.6.9
14h	WD_CONFIG_2(1)	Watchdog configuration 2	Section 10.6.10
15h	WD_INPUT_TRIG(1)	Watchdog input trigger	Section 10.6.11
16h	WD_RST_PULSE(1)	Watchdog output pulse width	Section 10.6.12
17h	FSM_CONFIG	Fail safe mode configuration	Section 10.6.13
18h	FSM_CNTR	Fail safe mode counter	Section 10.6.14
19h	DEVICE_RST	Device reset	Section 10.6.15
1Ah	DEVICE_CONFIG1	Device configuration	Section 10.6.16
1Bh	DEVICE_CONFIG2	Device configuration	Section 10.6.17
1Ch	SWE_DIS	Sleep wake error timer disable	Section 10.6.18
29h	SDO_CONFIG	Enables SDO to also support the nINT function	Section 10.6.19
2Dh	WD_QA_CONFIG	Q and A Watchdog configuration	Section 10.6.20
2Eh	WD_QA_ANSWER	Q and A Watchdog answer	Section 10.6.21
2Fh	WD_QA_QUESTION	Q and A Watchdog question	Section 10.6.22
30h	SW_ID1(2)	Selective wake ID 1	Section 10.6.23
31h	SW_ID2(2)	Selective wake ID 2	Section 10.6.24
32h	SW_ID3(2)	Selective wake ID 3	Section 10.6.25
33h	SW_ID4(2)	Selective wake ID 4	Section 10.6.26
34h	SW_ID_MASK1(2)	Selective wake ID mask 1	Section 10.6.27
35h	SW_ID_MASK2(2)	Selective wake ID mask 2	Section 10.6.28
36h	SW_ID_MASK3(2)	Selective wake ID mask 3	Section 10.6.29
37h	SW_ID_MASK4(2)	Selective wake ID mask 4	Section 10.6.30
38h	SW_ID_MASK_DLC(2)	ID Mask, DLC and Data mask enable	Section 10.6.31
39h + formula	DATA_y(2)	CAN data byte 7 through 0	Section 10.6.32
41h + formula	SW_RSVD_y(2)	SW_RSVD0 through SW_RSVD4	Section 10.6.33
44h	SW_CONFIG_1(2)	CAN and CAN FD DR and behavior	Section 10.6.34
45h	SW_CONFIG_2(2)	Frame counter	Section 10.6.35
46h	SW_CONFIG_3(2)	Frame counter threshold	Section 10.6.36

Table 10-19. Device Registers (continued)

Address	Acronym	Register Name	Section
47h	SW_CONFIG_4(2)	Mode configuration	Section 10.6.37
48h + formula	SW_CONFIG_RSVD_y(2)	SW_CONFIG_RSVD0 through SW_CONFIG_RSVD4	Section 10.6.38
50h	INT_GLOBAL	Global Interrupts	Section 10.6.39
51h	INT_1	Interrupts	Section 10.6.40
52h	INT_2	Interrupts	Section 10.6.41
53h	INT_3	Interrupts	Section 10.6.42
54h	INT_CANBUS(1)	CAN Bus fault interrupts	Section 10.6.43
55h	INT_GLOBAL_ENABLE	Interrupt enable for INT_GLOBAL	Section 10.6.44
56h	INT_ENABLE_1	Interrupt enable for INT_1	Section 10.6.45
57h	INT_ENABLE_2	Interrupt enable for INT_2	Section 10.6.46
58h	INT_ENABLE_3	Interrupt enable for INT_3	Section 10.6.47
59h	INT_ENABLE_CANBUS(1)	Interrupt enable for INT_CANBUS	Section 10.6.48
5Ah + formula	INT_RSVD_y	Interrupt Reserved Register INT_RSVD0 through INT_RSVD5	Section 10.6.49

(1) TCAN1144-Q1 and TCAN1146-Q1
(2) TCAN1145-Q1 and TCAN1146-Q1

Complex bit access types are encoded to fit into small table cells. Table 10-20 shows the codes that are used for access types in this section.

Table 10-20. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	H R	Set or cleared by hardware Read
Write Type		
H	H	Set or cleared by hardware
W	W	Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

10.6.1 DEVICE_ID_y Register (Address = 0h + formula) [reset = value]

DEVICE_ID_y is shown in Figure 10-40 and described in Table 10-21.

Return to Summary Table.

Device Part Number - reset value described in description field.

Offset = 0h + y; where y = 0h to 7h

Figure 10-40. DEVICE_ID_y Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-value							

Table 10-21. DEVICE_ID_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	value	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address Address 00h = 54h = T Address 01h = 43h = C Address 02h = 41h = A Address 03h = 4Eh = N Address 04h = 31h = 1 Address 05h = 31h = 1 Address 06h = 34h = 4 Address 07h = 34h = 4 for TCAN1144-Q1 Address 07h = 35h = 5 for TCAN1145-Q1 Address 07h = 36h = 6 for TCAN1146-Q1

10.6.2 REV_ID_MAJOR Register (Address = 8h) [reset = 01h]

REV_ID_MAJOR is shown in Figure 10-41 and described in Table 10-22.

Return to Summary Table.

Major Revision

Figure 10-41. REV_ID_MAJOR Register

7	6	5	4	3	2	1	0
Major_Revision							
R-01h							

Table 10-22. REV_ID_MAJOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Major_Revision	R	01h	Major die revision

10.6.3 REV_ID_MINOR Register (Address = 9h) [reset = 00h]

REV_ID_MINOR is shown in Figure 10-42 and described in Table 10-23.

Return to Summary Table.

Minor Revision

Figure 10-42. REV_ID_MINOR Register

7	6	5	4	3	2	1	0
Minor_Revision							
R-00h							

Table 10-23. REV_ID_MINOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Minor_Revision	R	00h	Minor die revision

10.6.4 SPI_RSVD_x Register (Address = Ah + formula) [reset = 00h]

SPI_RSVD_x is shown in Figure 10-43 and described in Table 10-24.

Return to Summary Table.

Configuration Reserved Bits Ah to Eh

Offset = Ah + x; where x = 0h to 4h

Figure 10-43. SPI_RSVD_x Register

7	6	5	4	3	2	1	0
SPI_RSVD_x							
R-00h							

Table 10-24. SPI_RSVD_x Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPI_RSVD_x	R	0b	SPI reserved registers 0 - 4

10.6.5 Scratch_Pad_SPI Register (Address = Fh) [reset = 00h]

Scratch_Pad_SPI is shown in Figure 10-44 and described in Table 10-25.

Return to Summary Table.

Read and Write Test Register SPI

Figure 10-44. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-00h							

Table 10-25. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	00h	Read and Write Test Register SPI

10.6.6 MODE_CNTRL Register (Address = 10h) [reset = 04h]

MODE_CNTRL is shown in Figure 10-45 and described in Table 10-26.

Return to Summary Table.

Mode select and feature enable and disable register

Figure 10-45. MODE_CNTRL Register

7	6	5	4	3	2	1	0
SW_EN	DTO_DIS	FD_EN	RSVD			MODE_SEL	
R/W-0b	R/W-0b	R/W-0b	R-00b			R/W-100b	

Table 10-26. MODE_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_EN	R/W	0b	Selective wake enable for TCAN1145-Q1 and TCAN1146-Q1 otherwise reserved 0b = Disabled 1b = Enabled

Table 10-26. MODE_CNTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DTO_DIS	R/W	0b	Disables dominant time out function 0b = Enabled 1b = Disabled
5	FD_EN	R/W	0b	CAN bus fault detection enable for TCAN1144-Q1 and TCAN1146-Q1 otherwise reserved 0b = Disabled 1b = Enabled
4-3	RSVD	R	00b	Reserved
2-0	MODE_SEL	R/W	100b	Mode of operation select 001b = Sleep 100b = Standby 101b = Listen 111b = Normal **Note** NOTE: The current mode will be read back and all other values are reserved

10.6.7 WAKE_PIN_CONFIG Register (Address = 11h) [reset = 4h]

WAKE_PIN_CONFIG is shown in Figure 10-46 and described in Table 10-27.

Return to Summary Table.

Register to configure the behavior of the WAKE pin.

Figure 10-46. WAKE_PIN_CONFIG Register

7	6	5	4	3	2	1	0
WAKE_CONFIG		WAKE_STAT		WAKE_WIDTH_INVALID		WAKE_WIDTH_MAX	
R/W-00b		R/W0C/H-00b		R/W-01b		R/W-00b	

Table 10-27. WAKE_PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	Wake pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Pulse
5-4	WAKE_STAT	R/W0C/H	00b	Status of the WAKE pin 00b = No change 01b = Rising edge 10b = Falling edge 11b = Pulse **Note** The status of the WAKE pin is displayed here after a state change. 00 must be written to these bits to clear the change. For Filtered WAKE Rising or falling edge will be displayed depending upon selected method from register 12h[7]
3-2	WAKE_WIDTH_INVALID	R/W	01b	Pulses less than or equal to these pulses are considered invalid 00b = 5 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 10 ms 01b = 10 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 20 ms 10b = 20 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 40 ms 11b = 40 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 80 ms

Table 10-27. WAKE_PIN_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	WAKE_WIDTH_MAX	R/W	00b	Maximum WAKE pin input pulse width to be considered valid. 00b = 750 ms 01b = 1000 ms 10b = 1500 ms 11b = 2000 ms

10.6.8 PIN_CONFIG Register (Address = 12h) [reset = 00h]

PIN_CONFIG is shown in Figure 10-47 and described in Table 10-28.

Return to Summary Table.

Device configuration register

Figure 10-47. PIN_CONFIG Register

7	6	5	4	3	2	1	0
WAKE_PULSE_CONFIG	RSVD		nINT_SEL		RXD_WK_CONFIG	RSVD	
R/W-0b	R-00b		R/W-00b		R/W-0b	R-00b	

Table 10-28. PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE_PULSE_CONFIG	R/W	0b	Set WAKE pin expected pulse/filtered direction 0b = Low –> High –> Low (Pulse), Low –> High (Filtered) 1b = High –> Low –> High (Pulse), High –> Low (Filtered)
6-5	RSVD	R	00b	Reserved
4-3	nINT_SEL	R/W	00b	nINT configuration selection: active low 00b = Global Interrupt 01b = Watchdog failure output 10b = Bus Fault Interrupt 11b = Wake Request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	RSVD	R	00b	Reserved

10.6.9 WD_CONFIG_1 Register (Address = 13h) [reset = 15h]

WD_CONFIG_1 is shown in Figure 10-48 and described in Table 10-29.

Return to Summary Table.

Watchdog configuration setup 1 for TCAN1144-Q1 and TCAN1146-Q1

Figure 10-48. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		WD_ERR_CNT_SET		WD_ACT	
R/W-00b		R/W-01b		R/W-01b		R/W-01b	

Table 10-29. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	00b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Q&A

Table 10-29. WD_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	WD_PRE	R/W	01b	Watchdog prescaler 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3-2	WD_ERR_CNT_SET	R/W	01b	Sets the watchdog event error counter that upon overflow the watchdog output will trigger 00b = Immediate trigger on each WD event 01b = Triggers on the fifth error event 10b = Triggers on the ninth error event 11b = Triggers on the 15th error event
1-0	WD_ACT	R/W	01b	Watchdog output trigger event action 00b = Turns off INH for 300 ms and sets WD interrupt 01b = Sets WD interrupt 10b = Reserved 11b = Reserved

10.6.10 WD_CONFIG_2 Register (Address = 14h) [reset = 02h]

WD_CONFIG_2 is shown in Figure 10-49 and described in Table 10-30.

Return to Summary Table.

Watchdog configuration setup 2 for TCAN1144-Q1 and TCAN1146-Q1

Figure 10-49. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				RSVD
R/W-000b			RH-0001b				R-0b

Table 10-30. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	000b	Sets window or timeout times based upon the WD_PRE setting See WD_TIMER table
4-1	WD_ERR_CNT	RH	0001b	Watchdog error counter Running count of errors up to 15 errors
0	RSVD	R	0b	Reserved

10.6.11 WD_INPUT_TRIG Register (Address = 15h) [reset = 00h]

WD_INPUT_TRIG is shown in Figure 10-50 and described in Table 10-31.

Return to Summary Table.

Writing FFh resets WD timer if accomplished at appropriate time for TCAN1144-Q1 and TCAN1146-Q1

Figure 10-50. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
W1C-00h							

Table 10-31. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

10.6.12 WD_RST_PULSE Register (Address = 16h) [reset = 07h]

WD_RST_PULSE is shown in Figure 10-51 and described in Table 10-32.

Return to Summary Table.

Selects the pulse width of the WD trigger event if nINT is selected for this function for TCAN1144-Q1 and TCAN1146-Q1

Figure 10-51. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
RESERVED				WDPW			
R-0000b				R/W-0111b			

Table 10-32. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved
3-0	WDPW	R/W	0111b	Window WD reset pulse width (ms) when selected 0001b = 3.6 - 5 0010b = 10 - 12.5 0100b = 40 - 50 0111b = 150 - 190 1000b = 1 - 1.5 1011b = 20 - 25 1101b = 60 - 75 1110b = 100 - 125

10.6.13 FSM_CONFIG Register (Address = 17h) [reset = 00h]

FSM_CONFIG is shown in Figure 10-52 and described in Table 10-33.

Return to Summary Table.

Configures the fail-safe mode

Figure 10-52. FSM_CONFIG Register

7	6	5	4	3	2	1	0
FS_CNTR_EN	FS_CNTR_ACT			FS_STAT			FS_DIS
R/W-0b	R/W-000b			RH-000b			R/W-0b

Table 10-33. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FS_CNTR_EN	R/W	0b	Enabled fail safe mode counter 0b = Disabled 1b = Enabled
6-4	FS_CNTR_ACT	R/W	000b	Action if fail safe counter exceeds programmed value 000b = No action 001b = Pull INH low for 1 s 010b = Perform soft reset 011b = Perform hard reset - POR 100b = Stop responding to wake events and go to sleep until power cycle reset 101b = Reserved 110b = Reserved 111b = Reserved **Note** NOTE: When selecting 001b, 010b and 011b the SWE timer will start after action has taken place.

Table 10-33. FSM_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	FS_STAT	RH	000b	Reason for entering fail-safe mode 000b = Not in FS mode 001b = Thermal shut down event 010b = Reserved 011b = UV_{CC} All other combinations are reserved **Note** These values are held until cleared by writing 0h to FSM_CNTR_STAT
0	FS_DIS	R/W	0b	Fail safe disable: Excludes power up fail safe 0b = Enabled 1b = Disabled

10.6.14 FSM_CNTR Register (Address = 18h) [reset = 00h]

FSM_CNTR is shown in Figure 10-53 and described in Table 10-34.

Return to Summary Table.

Set fail-safe counter and status

Figure 10-53. FSM_CNTR Register

7	6	5	4	3	2	1	0
FSM_CNTR_SET				FSM_CNTR_STAT			
R/W-0h				RH-0h			

Table 10-34. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0h	Sets the number of times FS mode enters before action taken. Value is one less than the number of times FS mode is entered. Range is 0-15, representing entering fail-safe mode 1-16 times
3-0	FSM_CNTR_STAT	RH	0h	Reads back the number of time FSM has been entered in a row up to 15. Can be cleared by writing 0h.

10.6.15 DEVICE_RST Register (Address = 19h) [reset = 00h]

DEVICE_RST is shown in Figure 10-54 and described in Table 10-35.

Return to Summary Table.

Forces a soft or hard reset.

Figure 10-54. DEVICE_RST Register

7	6	5	4	3	2	1	0
RESERVED						SF_RST	HD_RST
R-000000b						R/W1C-0b	R/W1C-0b

Table 10-35. DEVICE_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00000b	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers return to default values while keeping INH on.

Table 10-35. DEVICE_RST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset when writing a 1. **Note** NOTE: This will set the PWRON interrupt flag.

10.6.16 DEVICE_CONFIG1 Register (Address = 1Ah) [reset = 00h]

DEVICE_CONFIG1 is shown in Figure 10-55 and described in Table 10-36

Return to Summary Table.

Enables SPI to work in sleep mode if VIO is available.

LIMP pin only active for TCAN1144-Q1 and TCAN1146-Q1 otherwise reserved for TCAN1145-Q1.

Figure 10-55. DEVICE_CONFIG1 Register

7	6	5	4	3	2	1	0
RSVD	INH_DIS	INH_LIMP_SEL	LIMP_DIS	LIMP_SEL_RESET		LIMP_RESET	RSVD
R-0b	R/W-0b	R/W - 0b	R/W - 0b	R/W - 00b		R/W1C - 0b	R - 0b

Table 10-36. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	INH_DIS	R/W	0b	INH pin disable 0b = Enabled 1b = Disabled
5	INH_LIMP_SEL	R/W	0b	Pin function select 0b = INH 1b = LIMP
4	LIMP_DIS	R/W	0b	LIMP pin disable if LIMP function selected 0b = Enabled 1b = Disabled
3-2	LIMP_SEL_RESET	R/W	00b	Selects the method to reset/turnoff the LIMP pin 00b = On third successful input trigger the error counter receives 01b = First correct input trigger 10b = SPI write to 8'h1A[1] = 1 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset/turn off: Writing a one to this location resets the LIMP pin to off state and bit automatically clears
0	RSVD	R	0b	Reserved

10.6.17 DEVICE_CONFIG2 Register (Address = 1Bh) [reset = 0h]

DEVICE_CONFIG2 is shown in Figure 10-56 and described in Table 10-37.

Return to Summary Table.

Disables the $t_{WK\_WIDTH\_MAX}$ from WAKE pin pulse configuration and makes the WAKE pin a filtered WAKE pin based off of $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$

Figure 10-56. DEVICE_CONFIG2 Register

7	6	5	4	3	2	1	0
RESERVED						WAKE_WIDTH_MAX_DIS	RSVD
R-00000b						R/W-0b	R-0b

Table 10-37. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00000b	Reserved
1	WAKE_WIDTH_MAX_DIS	R/W	0b	WAKE pulse maximum width disable. Disables $t_{WK\_WIDTH\_MAX}$ and puts the device into WAKE filtered configuration. 0b = Enabled 1b = Disabled
0	RSVD	R	0b	Reserved

10.6.18 SWE_DIS Register (Address 1Ch) [reset = 04h]

SWE_DIS is shown in Figure 10-57 and described in Table 10-38.

Return to Summary Table.

Disabled the sleep wake error timer. Does not disable the timer for power on.

Figure 10-57. SWE_DIS Register

7	6	5	4	3	2	1	0
SWE_DIS	RESERVED				CANSLNT_SWE_DIS	RESERVED	
R/W-0b	R-0000b				R/W-1b	R-00b	

Table 10-38. SWE_DIS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_DIS	R/W	0b	Sleep wake error disable: NOTE: This disables the device from starting the SWE timer when coming out of sleep mode on a wake event. If this is enabled a SPI read or write must take place within the SWE timer window or the device will go back to sleep. This does not disable the function for initial power on or in case of a power on reset. 0b = Enabled 1b = Disabled
6-3	RSVD	R	0000b	Reserved
2	CANSLNT_SWE_DIS	R/W	1b	SWE timer will be disabled from the CANSLNT flag and based only on $t_{Silence}$ 0b = Enabled 1b = Disabled
1-0	RSVD	R	00b	Reserved

10.6.19 SDO_CONFIG Register (Address = 29h) [reset = 00h]

SDO_CONFIG is shown in Figure 10-58 and described in Table 10-39.

Return to Summary Table.

Configures SDO pin as SDO only or allows the pin to also behave like an interrupt pin, nINT.

Figure 10-58. SDO_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED							SDO_CONFIG
R-0000000b							R/W-0b

Table 10-39. SDO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved

Table 10-39. SDO_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SDO_CONFIG	R/W	0b	SDO pin configuration: NOTE: When configured as SDO and nINT the pin will behave as SDO when nCS is low and will behave as nINT when nCS is high 0b = SDO only 1b = SDO and nINT

10.6.20 WD_QA_CONFIG Register (Address = 2Dh) [reset = 00h]

WD_QA_CONFIG is shown in Figure 10-59 and described in Table 10-40.

Return to Summary Table.

Q&A watchdog configuration bits

Figure 10-59. WD_QA_CONFIG Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG		WD_Q&A_POLY_CFG		WD_Q&A_POLY_SEED			
R/W-00b		R/W-00b		R/W-0000b			

Table 10-40. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_Q&A_POLY_CFG	R/W	00b	WD Q&A polynomial configuration
3-0	WD_Q&A_POLY_SEED	R/W	0000b	WD Q&A polynomial seed value loaded when device is in the RESET state

Note

Upon power up, WD_Q&A_POLY_SEED will read back 0000b but the actual seed value is 1010b. Once written to the read back value and actual value will be the same.

10.6.21 WD_QA_ANSWER Register (Address = 2Eh) [reset = 00h]

WD_QA_ANSWER is shown in Figure 10-60 and described in Table 10-41.

Return to Summary Table.

Q&A watchdog answer bits

Figure 10-60. WD_QA_ANSWER Register

7	6	5	4	3	2	1	0
WD_QA_ANSWER							
R-00h							

Table 10-41. WD_QA_ANSWER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W	00h	MCU watchdog Q&A answer response byte

10.6.22 WD_QA_QUESTION Register (Address = 2Fh) [reset = 00h]

WD_QA_QUESTION is shown in Figure 10-61 and described in Table 10-42.

Return to Summary Table.

Q&A watchdog question bits

Figure 10-61. WD_QA_QUESTION Register

7	6	5	4	3	2	1	0

Figure 10-61. WD_QA_QUESTION Register (continued)

RSVD	QA_ANSW_ERR	WD_ANSW_CNT	WD_QUESTION
R-0b	W1C-0b	R-00b	R-0000b

Table 10-42. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	QA_ANSW_ERR	W1C	0b	Watchdog Q&A answer error flag
5-4	WD_ANSW_CNT	R	00b	Current state of received Watchdog Q&A error counter When WD enabled value will show up as 2'h3
3-0	WD_QUESTION	R	0000b	Current watchdog question value When WD is enabled value will show up as 4'hC

10.6.23 SW_ID1 Register (Address = 30h) [reset = 00h]

SW_ID1 is shown in Figure 10-62 and described in Table 10-43.

Return to Summary Table.

Extended ID bits 17:10 for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-62. SW_ID1 Register

7	6	5	4	3	2	1	0
EXT_ID_17:10							
R/W-00h							

Table 10-43. SW_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_17:10	R/W	00h	Extended ID bits 17:10

10.6.24 SW_ID2 Register (Address = 31h) [reset = 00h]

SW_ID2 is shown in Figure 10-63 and described in Table 10-44.

Return to Summary Table.

Extended ID bits 9:2 for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-63. SW_ID2 Register

7	6	5	4	3	2	1	0
EXT_ID_9:2							
R/W-00h							

Table 10-44. SW_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_9:2	R/W	00h	Extended ID bits 9:2

10.6.25 SW_ID3 Register (Address = 32h) [reset = 00h]

SW_ID3 is shown in Figure 10-64 and described in Table 10-45.

Return to Summary Table.

Extended ID bits 1:0, Extended ID Field, ID[10:6] and Extended ID[28:24] for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-64. SW_ID3 Register

7	6	5	4	3	2	1	0
EXT_ID_1:0		IDE	ID_10:6__EXT_ID_28:24				

Figure 10-64. SW_ID3 Register (continued)

R/W-00b	R/W-0b	R/W-00000b

Table 10-45. SW_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EXT_ID_1:0	R/W	00b	Extended ID bits 1:0
5	IDE	R/W	0b	Extended ID field 0b = Standard ID (11-bits) 1b = Extended ID (29-bits)
4-0	ID_10:6__EXT_ID_28:24	R/W	00000b	ID[10:6] and Extended ID[28:24]

10.6.26 SW_ID4 Register (Address = 33h) [reset = 00h]

SW_ID4 is shown in Figure 10-65 and described in Table 10-46.

Return to Summary Table.

ID[5:0] and Extended ID[23:18] for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-65. SW_ID4 Register

7	6	5	4	3	2	1	0
ID_5:0__EXT_ID_23:18						RESERVED	
R/W-000000b						R-00b	

Table 10-46. SW_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ID_5:0__EXT_ID_23:18	R/W	000000b	ID[5:0] and Extended ID[23:18]
1-0	RESERVED	R	00b	Reserved

10.6.27 SW_ID_MASK1 Register (Address = 34h) [reset = 00h]

SW_ID_MASK1 is shown in Figure 10-66 and described in Table 10-47.

Return to Summary Table.

Extended ID Mask 17:16 for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-66. SW_ID_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED						EXT_ID_MASK_17:16	
R-000000b						R/W-00b	

Table 10-47. SW_ID_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1-0	EXT_ID_MASK_17:16	R/W	00b	Extended ID Mask 17:16

10.6.28 SW_ID_MASK2 Register (Address = 35h) [reset = 00h]

SW_ID_MASK2 is shown in Figure 10-67 and described in Table 10-48.

Return to Summary Table.

Extended ID Mask 15:8 for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-67. SW_ID_MASK2 Register

7	6	5	4	3	2	1	0
EXT_ID_MASK_15:8							

Figure 10-67. SW_ID_MASK2 Register (continued)

R/W-00h

Table 10-48. SW_ID_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_15:8	R/W	00h	Extended ID Mask 15:8

10.6.29 SW_ID_MASK3 Register (Address = 36h) [reset = 00h]

SW_ID_MASK3 is shown in Figure 10-68 and described in Table 10-49.

Return to Summary Table.

Extended ID Mask 7:0 for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-68. SW_ID_MASK3 Register

7	6	5	4	3	2	1	0
EXT_ID_MASK_7:0							
R/W-00h							

Table 10-49. SW_ID_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_7:0	R/W	00h	Extended ID Mask 7:0

10.6.30 SW_ID_MASK4 Register (Address = 37h) [reset = 00h]

SW_ID_MASK4 is shown in Figure 10-69 and described in Table 10-50.

Return to Summary Table.

ID Mask 10:3 and Extended ID Mask 28:21 (Base ID) for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-69. SW_ID_MASK4 Register

7	6	5	4	3	2	1	0
ID_MASK_10:3__EXT_ID_MASK_28:21							
R/W-00h							

Table 10-50. SW_ID_MASK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ID_MASK_10:3__EXT_ID_MASK_28:21	R/W	00h	ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

10.6.31 SW_ID_MASK_DLC Register (Address = 38h) [reset = 00h]

SW_ID_MASK_DLC is shown in Figure 10-70 and described in Table 10-51.

Return to Summary Table.

ID Mask 2:0 and Extended ID Mask 20:18 (Base ID), DLC[3:0], Data mask enable for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-70. SW_ID_MASK_DLC Register

7	6	5	4	3	2	1	0
SW_ID_MASK_5			DLC				DATA_MASK_EN
R/W-000b			R/W-0000b				R/W-0b

Table 10-51. SW_ID_MASK_DLC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SW_ID_MASK_5	R/W	000b	ID Mask 2:0 and Extended ID Mask 20:18 (Base ID)
4-1	DLC	R/W	0000b	DLC[3:0]
0	DATA_MASK_EN	R/W	0b	Data mask enable 0b = DLC field and Data field are not compared and assumed valid. Remote frames are allowed. 1b = DLC field must match DLC[3:0] register and data field bytes are compared with DATAx registers for a matching 1. Remote frames are ignored

10.6.32 DATA_y Register (Address = 39h + formula) [reset = 00h]

DATA_y is shown in Figure 10-71 and described in Table 10-52.

Return to Summary Table.

Register address 39h through 40h

Offset = 39h + (y * 1h); where y = 0h to 7h for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-71. DATA_y Register

7	6	5	4	3	2	1	0
DATAx							
R/W-00h							

Table 10-52. DATA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATAx	R/W	00h	CAN data byte x

10.6.33 SW_RSVD_y Register (Address = 41h + formula) [reset = 00h]

SW_RSVD_y is shown in Figure 10-72 and described in Table 10-53.

Return to Summary Table.

Register address 41h through 43F

Offset = 41h + (y * 1h); where y = 0h to 2h for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-72. SW_RSVD_y Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-53. SW_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

10.6.34 SW_CONFIG_1 Register (Address = 44h) [reset = 50h]

SW_CONFIG_1 is shown in Figure 10-73 and described in Table 10-54.

Return to Summary Table.

CAN and CAN FD DR and Behavior for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-73. SW_CONFIG_1 Register

7	6	5	4	3	2	1	0
SW_FD_PASSIVE	CAN_DR			FD_DR		RSVD	

Figure 10-73. SW_CONFIG_1 Register (continued)

R/W-0b	R/W-101b	R/W-00b	R-00b

Table 10-54. SW_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_FD_PASSIVE	R/W	0b	Selective Wake FD Passive: this bit modifies the behavior of the error counter when CAN with flexible data rate frames are seen. 0b = CAN with flexible data rate frame will be counted as an error frame 1b = CAN with flexible data rate frame are ignored (passive)
6-4	CAN_DR	R/W	101b	CAN bus data rate 000b = 50 Kbps 001b = 100 Kbps 010b = 125 Kbps 011b = 250 Kbps 100b = Reserved 101b = 500 Kbps 110b = Reserved 111b = 1 Mbps
3-2	FD_DR	R/W	00b	CAN bus FD data rate ratio verses CAN data rate 00b = CAN FD <= 4x CAN data rate 01b = CAN FD => 5x and <= 10x CAN data rate 10b = Reserved 11b = Reserved
1-0	RSVD	R	0b	Reserved

10.6.35 SW_CONFIG_2 Register (Address = 45h) [reset = 00h]

SW_CONFIG_2 is shown in Figure 10-74 and described in Table 10-55.

Return to Summary Table for TCAN1145-Q1 and TCAN1146-Q1.

Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame will have no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment will overflow the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

Figure 10-74. SW_CONFIG_2 Register

7	6	5	4	3	2	1	0
FRAME_CNTx							
RH-00h							

Table 10-55. SW_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNTx	RH	00h	Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame will have no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment will overflow the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

10.6.36 SW_CONFIG_3 Register (Address = 46h) [reset = 1Fh]

SW_CONFIG_3 is shown in Figure 10-75 and described in Table 10-56.

Return to Summary Table.

Frame Error Counter Threshold: these bits set the point at which the error counter reaches its maximum and on the next error frame will overflow and set the FRAME_OVF flag. Default is 31 so the 32nd error will set the overflow flag for TCAN1145-Q1 and TCAN1146-Q1.

Figure 10-75. SW_CONFIG_3 Register

7	6	5	4	3	2	1	0
FRAME_CNT_THRESHOLD							
R/W-1Fh							

Table 10-56. SW_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNT_THRESHOLD	R/W	1Fh	Frame Error Counter Threshold: these bits set the point at which the error counter reaches its maximum and on the next error frame will overflow and set the FRAME_OVF flag. Default is 31 so the 32nd error will set the overflow flag.

10.6.37 SW_CONFIG_4 Register (Address = 47h) [reset = 00h]

SW_CONFIG_4 is shown in Figure 10-76 and described in Table 10-57.

Return to Summary Table.

Configuration for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-76. SW_CONFIG_4 Register

7	6	5	4	3	2	1	0
SWCFG	CAN_SYNC_FD	CAN_SYNC	RSVD				
RH/W-0b	RH-0b	RH-0b	R-00000b				

Table 10-57. SW_CONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWCFG	RH/W	0b	Selective wake configuration complete 0b = SW registers not configured 1b = SW registers configured Note: Make this the last step in configuring and turning on selective wake. **Note** NOTE: Writing to any of these wake configuration registers (8'h30-8'h44, 8'h46) clears the SWCFG bit.
6	CAN_SYNC_FD	RH	0b	Device is properly decoding CAN FD frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system may determine if the device is properly decoding CAN FD frames, up to but not including the Data Field. This flag is self-clearing.
5	CAN_SYNC	RH	0b	Synchronized to CAN data: this flag indicates if the device is properly decoding CAN frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag the system may determine if the device is properly decoding CAN frames. This flag is self-clearing.
4-0	RSVD	R	00000b	Reserved

10.6.38 SW_CONFIG_RSVD_y Register (Address = 48h + formula) [reset = 00h]

SW_CONFIG_RSVD_y is shown in Figure 10-77 and described in Table 10-58.

Return to Summary Table.

Register address 48h through 4Fh

Offset = 48h + (y * 1h); where y = 0h to 7h for TCAN1145-Q1 and TCAN1146-Q1

Figure 10-77. SW_CONFIG_RSVD_y Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-58. SW_CONFIG_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

10.6.39 INT_GLOBAL Register (Address = 50h) [reset = 00h]

INT_GLOBAL is shown in Figure 10-78 and described in Table 10-59.

Return to Summary Table.

Logical OR of all to certain interrupts

Figure 10-78. INT_GLOBAL Register

7	6	5	4	3	2	1	0
GLOBALERR	INT_1	INT_2	INT_3	INT_CANBUS	RSVD		
RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	R-000b		

Table 10-59. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBALERR	RH	0b	Logical OR of all interrupts
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	1b	Logical OR of INT_2 register
4	INT_3	RH	0b	Logical OR of INT_3 register
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2-0	RSVD	R	0000b	Reserved

10.6.40 INT_1 Register (Address = 51h) [reset = 00h]

INT_1 is shown in Figure 10-79 and described in Table 10-60.

Return to Summary Table.

Interrupts are dependent on device. All interrupts are for TCAN1146-Q1. Watchdog and CAN bus interrupts are for TCAN1144-Q1. Selective wake interrupts are for TCAN1145-Q1

Figure 10-79. INT_1 Register

7	6	5	4	3	2	1	0
WD	CANINT	LWU	WKERR	FRAME_OVF	CANSLNT	CANTO	CANDOM
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-60. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. **Note** This interrupt bit will be set for every watchdog error event and does not rely upon the Watchdog error counter

Table 10-60. INT_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CANINT	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	FRAME_OVF	R/W1C	0b	Frame error counter overflow
2	CANSLNT	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$
1	CANTO	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$ while Selective Wake is enabled and in Sleep mode
0	CANDOM	R/W1C	0b	CAN bus stuck dominant

10.6.41 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in Figure 10-80 and described in Table 10-61.

Return to Summary Table.

Interrupts All interrupts are for TCAN1146-Q1. Watchdog and CAN bus interrupts are for TCAN1144-Q1. Selective wake interrupts are for TCAN1145-Q1

Figure 10-80. INT_2 Register

7	6	5	4	3	2	1	0
SMS	PWRON	RSVD	UVSUP	UVIO	UVCC	TSD	TSDW
R/W1C-0b	R/W1C-1b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-61. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Only sets when sleep mode is entered by a WKERR, UVIO timeout or UVIO + TSD fault
6	PWRON	R/W1C	1b	Power on
5	RSVD	R-0b	0b	Reserved
4	UVSUP	R/W1C	0b	V_{SUP} under voltage
3	UVIO	R/W1C	0b	V_{IO} under voltage
2	UVCC	R/W1C	0b	V_{CC} under voltage
1	TSD	R/W1C	0b	Thermal Shutdown
0	TSDW	R/W1C	0b	Thermal Shutdown Warning

10.6.42 INT_3 Register (Address 53h) [reset = 00h]

INT_3 is shown in Figure 10-81 and described in Table 10-62.

Return to Summary Table.

All interrupts are for TCAN1146-Q1. Watchdog and CAN bus interrupts are for TCAN1144-Q1. Selective wake interrupts are for TCAN1145-Q1

The CRC_EEPROM interrupt is set when the internal EEPROM used for trimming has a CRC error. Upon power-up, the device loads an internal register from the EEPROM and performs a CRC check. If an error is present after eight attempts of loading valid data the CRC_EEPROM interrupt will be set. This will indicate an error that may impact device performance. This is repeated when the device leaves sleep mode or fail-safe mode due to a wake event. The device will perform a CRC check on the internal registers loaded from the EEPROM. If there is an error the device will reload the registers from the EEPROM. If there is a CRC error the device will attempt to load the internal registers up to eight times. After the eighth attempt the CRC_EEPROM interrupt flag will be set. This will indicate an error that may impact the device performance.

Figure 10-81. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	SWERR	FSM	RSVD				CRC_EEPROM
R/W1C-0b	RH-0b	R/W1C-0b	R-0000b				R/W1C-0b

Table 10-62. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	SWERR	RH	0b	Logical OR of (SW_EN=1 and NOT(SWCFG)) and FRAME_OVF. Selective Wake may not be enabled while SWERR is set
5	FSM	R/W1C	0b	Entered fail-safe mode. Can be cleared while in fail-safe mode.
4-1	RSVD	R	0000b	Reserved
0	CRC_EEPROM	R/W1C	0b	EEPROM CRC error

10.6.43 INT_CANBUS Register (Address = 54h) [reset = 00h]

INT_CANBUS is shown in Figure 10-82 and described in Table 10-63.

Return to Summary Table.

CAN bus faults that include shorts and opens for TCAN1144-Q1 and TCAN1146-Q1

Figure 10-82. INT_CANBUS Register

7	6	5	4	3	2	1	0
RSVD	CANBUSTERMOPEN	CANHCANL	CANHBAT	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSBAT
R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-63. INT_CANBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	CANBUSTERMOPEN	R/W1C	0b	CAN bus has one termination point open
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

10.6.44 INT_GLOBAL_ENABLE (Address = 55h) [reset = 00h]

INT_GLOBAL_ENABLE is shown in Figure 10-83 and described in Table 10-64.

Return to Summary Table.

Interrupt mask for Global interrupts

Figure 10-83. INT_GLOBAL_ENABLE Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-64. INT_GLOBAL_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

10.6.45 INT_ENABLE_1 Register (Address = 56h) [reset = FFh]

INT_ENABLE_1 is shown in Figure 10-84 and described in Table 10-65.

Return to Summary Table.

Interrupt masks for INT_1; All interrupt masks are for TCAN1146-Q1. Watchdog and CAN bus interrupt masks are for TCAN1144-Q1. Selective wake interrupt masks are for TCAN1145-Q1

Figure 10-84. INT_ENABLE_1 Register

7	6	5	4	3	2	1	0
WD_ENABLE	CANINT_ENABLE	LWU_ENABLE	WKERR_ENABLE	FRAME_OVF_ENABLE	CANSLNT_ENABLE	CANTO_ENABLE	CANDOM_ENABLE
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-65. INT_ENABLE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_ENABLE	R/W	1b	Watchdog event interrupt enable
6	CANINT_ENABLE	R/W	1b	CAN bus wake up interrupt enable
5	LWU_ENABLE	R/W	1b	Local wake up enable
4	WKERR_ENABLE	R/W	1b	Wake error enable
3	FRAME_OVF_ENABLE	R/W	1b	Frame error counter overflow enable
2	CANSLNT_ENABLE	R/W	1b	CAN silent enable
1	CANTO_ENABLE	R/W	1b	CAN timeout enable
0	CANDOM_ENABLE	R/W	1b	CAN bus stuck dominant enable

10.6.46 INT_ENABLE_2 Register (Address = 57h) [reset = 1Fh]

INT_ENABLE_2 is shown in Figure 10-85 and described in Table 10-66.

Return to Summary Table.

Interrupt masks for INT_2

Figure 10-85. INT_ENABLE_2 Register

7	6	5	4	3	2	1	0
RSVD			UVSUP_ENABLE	UVIO_ENABLE	UVCC_ENABLE	TSD_ENABLE	TSDW_ENABLE
R-000b			R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-66. INT_ENABLE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Reserved
4	UVSUP_ENABLE	R/W	1b	V_{SUP} under voltage enable
3	UVIO_ENABLE	R/W	1b	V_{IO} under voltage enable
2	UVCC_ENABLE	R/W	1b	V_{CC} under voltage enable
1	TSD_ENABLE	R/W	1b	Thermal shutdown enable
0	TSDW_ENABLE	R/W	1b	Thermal shutdown warning enable

10.6.47 INT_ENABLE_3 Register (Address = 58h) [reset = 0h]

INT_ENABLE_3 is shown in Figure 10-86 and described in Table 10-67.

Return to Summary Table.

Interrupt masks for INT_3; All interrupt masks are for TCAN1146-Q1. Watchdog and CAN bus interrupt masks are for TCAN1144-Q1. Selective wake interrupt masks are for TCAN1145-Q1

Figure 10-86. INT_ENABLE_3 Register

7	6	5	4	3	2	1	0
SPIERR_ENABLE	SWERR_ENABLE	FSM_ENABLE	RSVD				
R/W-1b	R/W-0b	R/W-1b	R-00000b				

Table 10-67. INT_ENABLE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_ENABLE	R/W	1b	SPI error interrupt enable
6	SWERR_ENABLE	R/W	0b	Selective wake error enable
5	FSM_ENABLE	R/W	1b	Fail-safe mode enable
4-0	RSVD	R	00000b	Reserved

10.6.48 INT_ENABLE_CANBUS Register (Address = 59h) [reset = 7Fh]

INT_ENABLE_CANBUS is shown in INT_ENABLE_CANBUS Register and described in INT_ENABLE_CANBUS Register Field Descriptions.

Return to Summary Table.

Interrupt masks for INT_CANBUS; for TCAN1144-Q1 and TCAN1146-Q1

Figure 10-87. INT_ENABLE_CANBUS Register

7	6	5	4	3	2	1	0
RESERVED	CANBUSTERMOPEN_ENABLE	CANHCANL_ENABLE	CANHBAT_ENABLE	CANLGND_ENABLE	CANBUSOPEN_ENABLE	CANBUSGND_ENABLE	CANBUSBAT_ENABLE
R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-68. INT_ENABLE_CANBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	CANBUSTERMOPEN_ENABLE	R/W	1b	CAN bus termination open enable
5	CANHCANL_ENABLE	R/W	1b	CANH and CANL shorted together enable
4	CANHBAT_ENABLE	R/W	1b	CANH shorted to Vbat enable
3	CANLGND_ENABLE	R/W	1b	CANL shorted to GND enable
2	CANBUSOPEN_ENABLE	R/W	1b	CAN bus open enable
1	CANBUSGND_ENABLE	R/W	1b	CAN bus shorted to GND enable
0	CANBUSBAT_ENABLE	R/W	1b	CAN bus shorted to Vbat enable

10.6.49 INT_RSVD_y Register (Address = 5Ah + formula) [reset = 00h]

INT_RSVD_y is shown in Figure 10-88 and described in Table 10-69.

Return to Summary Table.

Register address 58h through 5Fh

Offset = 58h + (y * 1h); where y = 0h to 7h

Figure 10-88. INT_RSVD_y Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-69. INT_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

11 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

11.1.1 BUS Loading, Length and Number of Nodes

The ISO 11898-2:2016 standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as this transceiver family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2016 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In ISO 11898-2:2016 the driver differential output is specified with a 60 Ω bus load (the two termination resistors in parallel) where the differential output must be greater than 1.5 V. The TCAN114x-Q1 is specified to meet the 1.5 V requirement with a across this load range and is specified to meet 1.4 V differential output at 45 Ω bus load. The differential input resistance of this family of transceiver is a minimum of 30 kΩ. If 167 of these transceivers are in parallel on a bus, this is equivalent to a 180 Ω differential load in parallel with the 60 Ω from termination gives a total bus load of 45 Ω. Therefore, this family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2 V minimum differential input voltage requirements at each receiving node. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond the original ISO 11898-2:2016 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO 11898-2:2016 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

11.1.2 CAN Termination

The ISO 11898-2:2016 standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (ZO).

11.1.2.1 Termination

Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

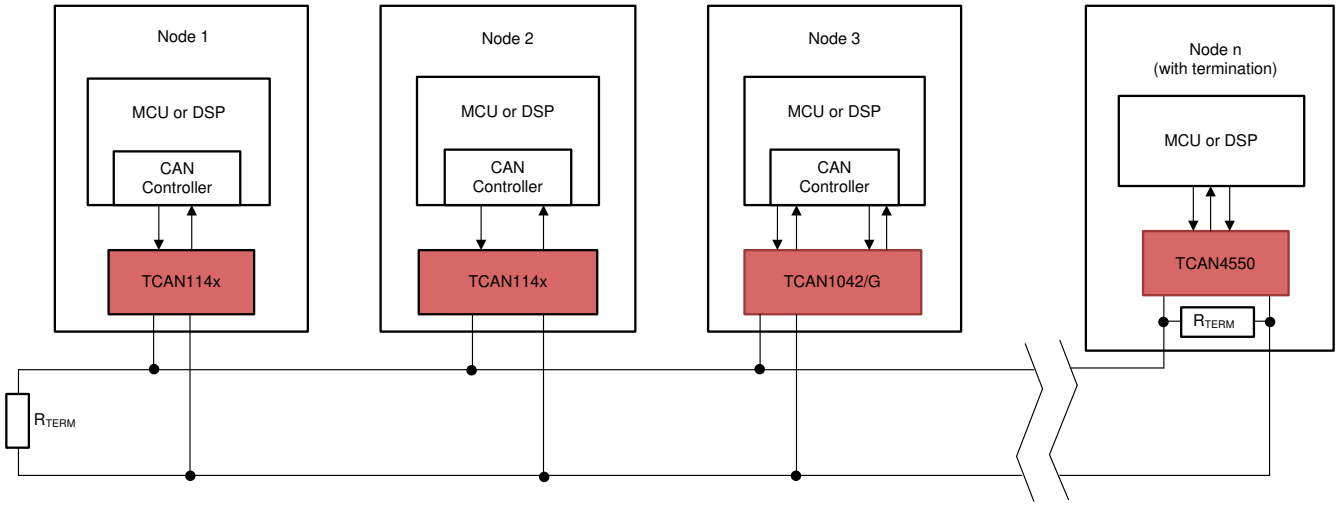


Figure 11-1. Typical CAN Bus

Termination may be a single 120 Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” may be used, see Figure 11-2. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

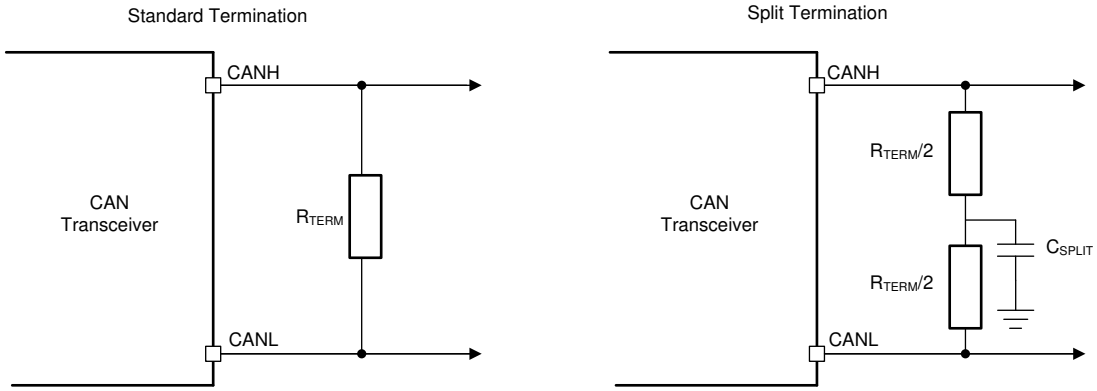


Figure 11-2. CAN Bus Termination Concepts

11.1.2.2 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 11-3 for the state diagram on how the TCAN114x-Q1 performs automatic biasing.

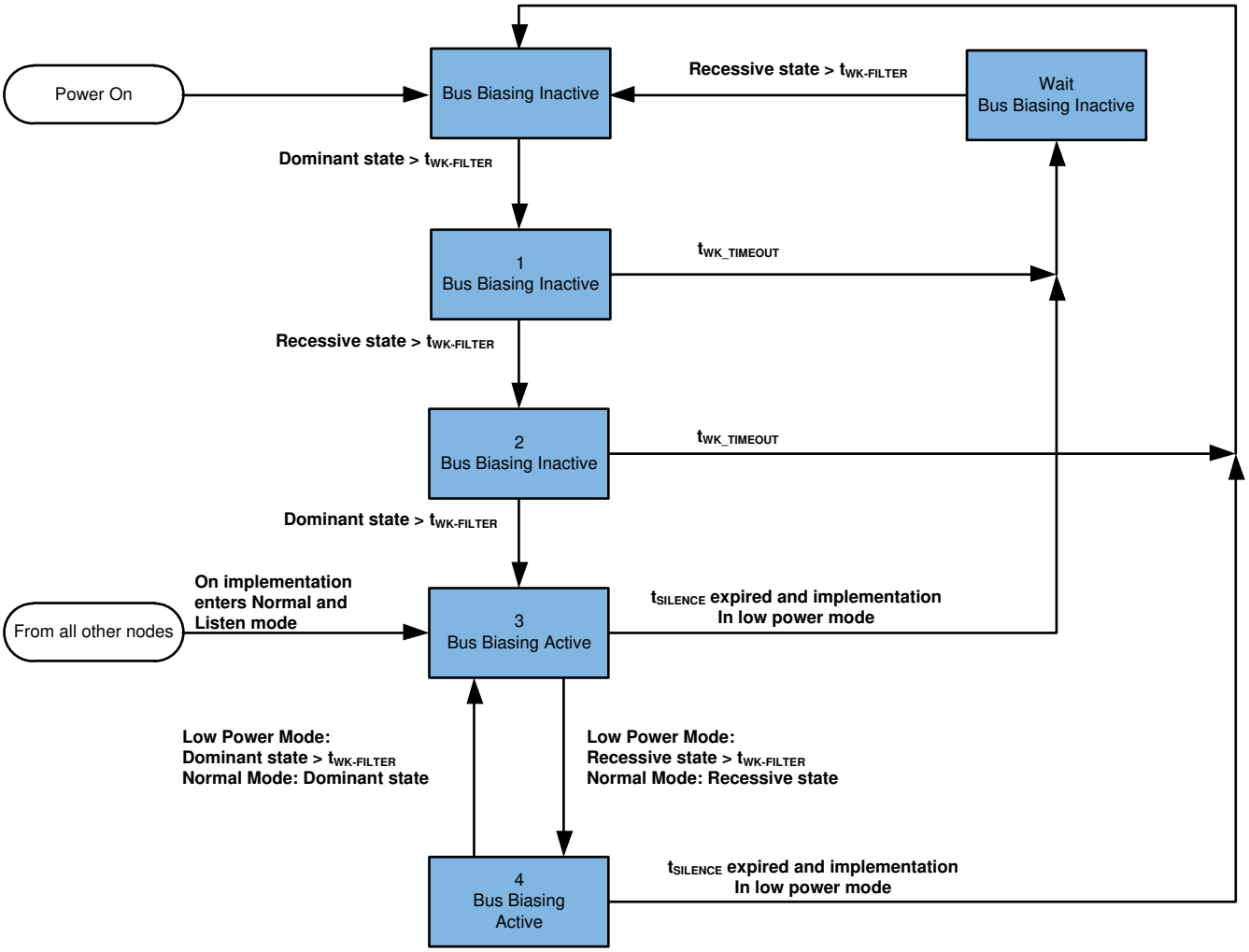


Figure 11-3. Automatic bus biasing state diagram

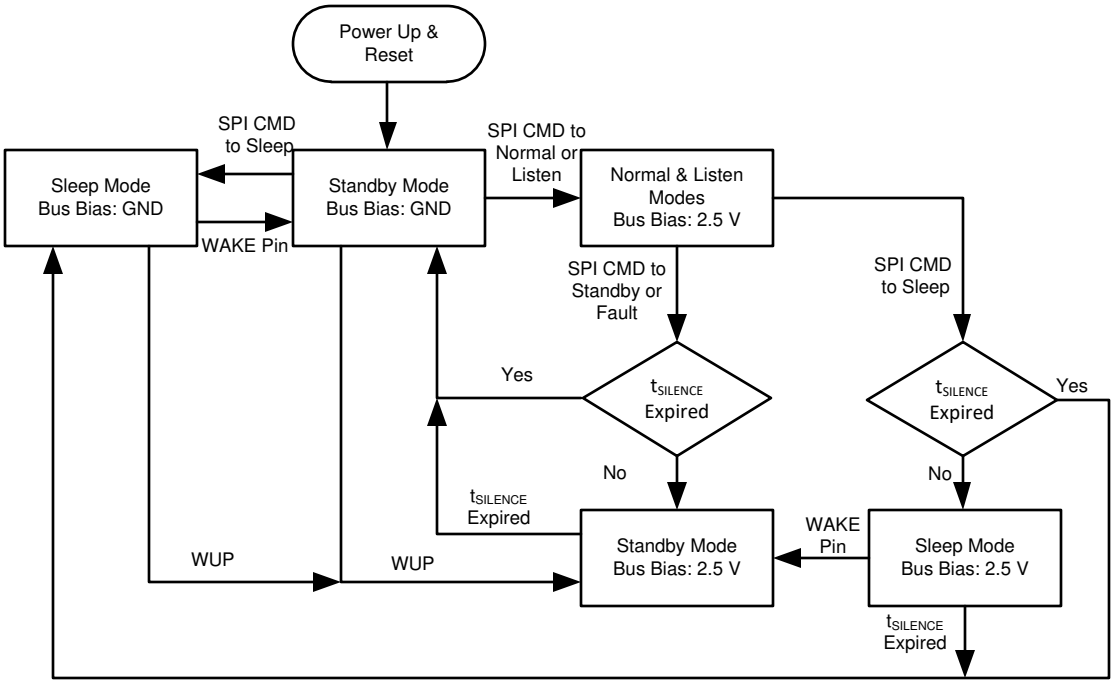


Figure 11-4. Bus biasing by Mode

Note

Fail-safe, TSD and VIO protected modes follow automatic bus biasing similar to Standby mode.

11.2 Typical Application

The TCAN114x-Q1 is typically used as the CAN FD transceiver in applications where the host microprocessor or FPGA supporting a CAN controller does not have an integrated CAN transceiver. Below is a typical application configuration for 3.3 V microprocessor applications. The TCAN114x-Q1 works with 3.3 V and 5 V microprocessors when using the V_{IO} pin from the microprocessor voltage regulator. The bus termination is shown for illustrative purposes.

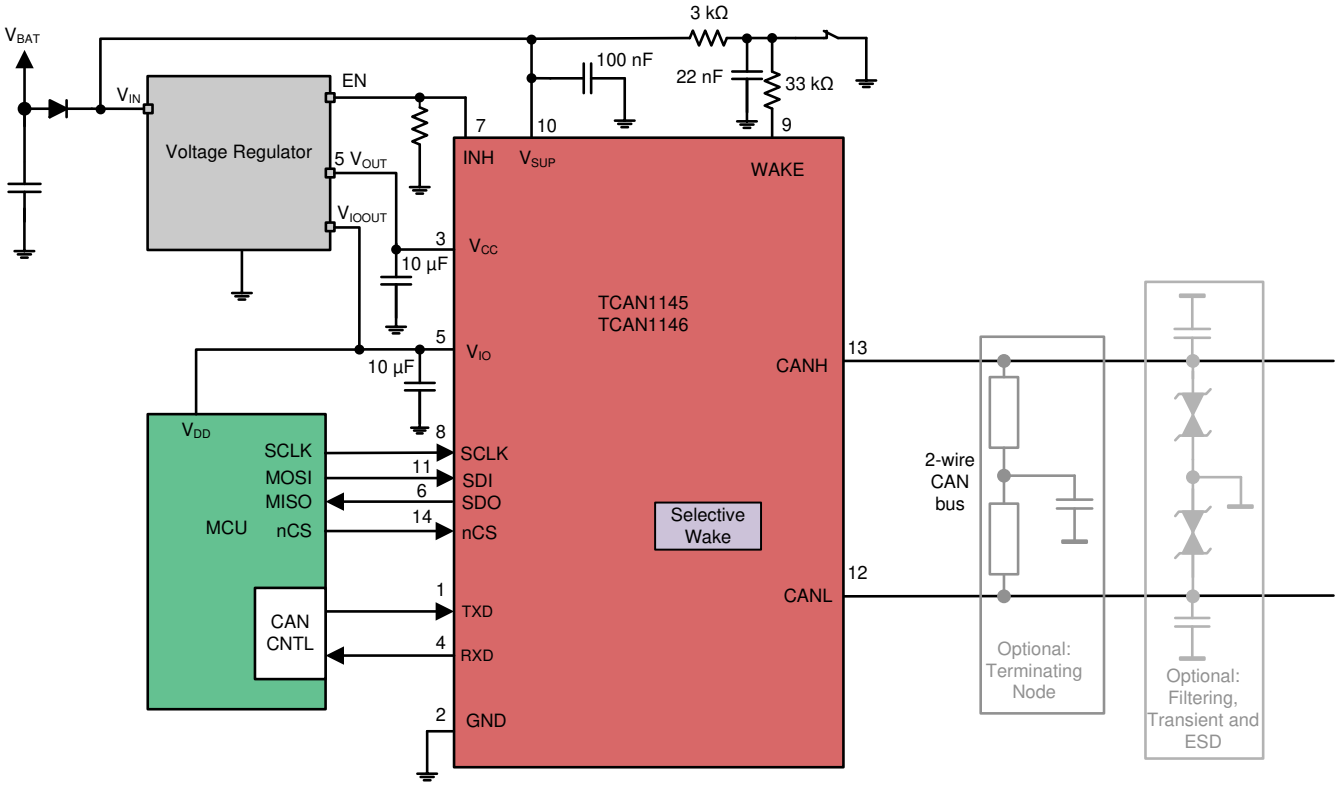


Figure 11-5. Typical CAN Applications for TCAN114x-Q1

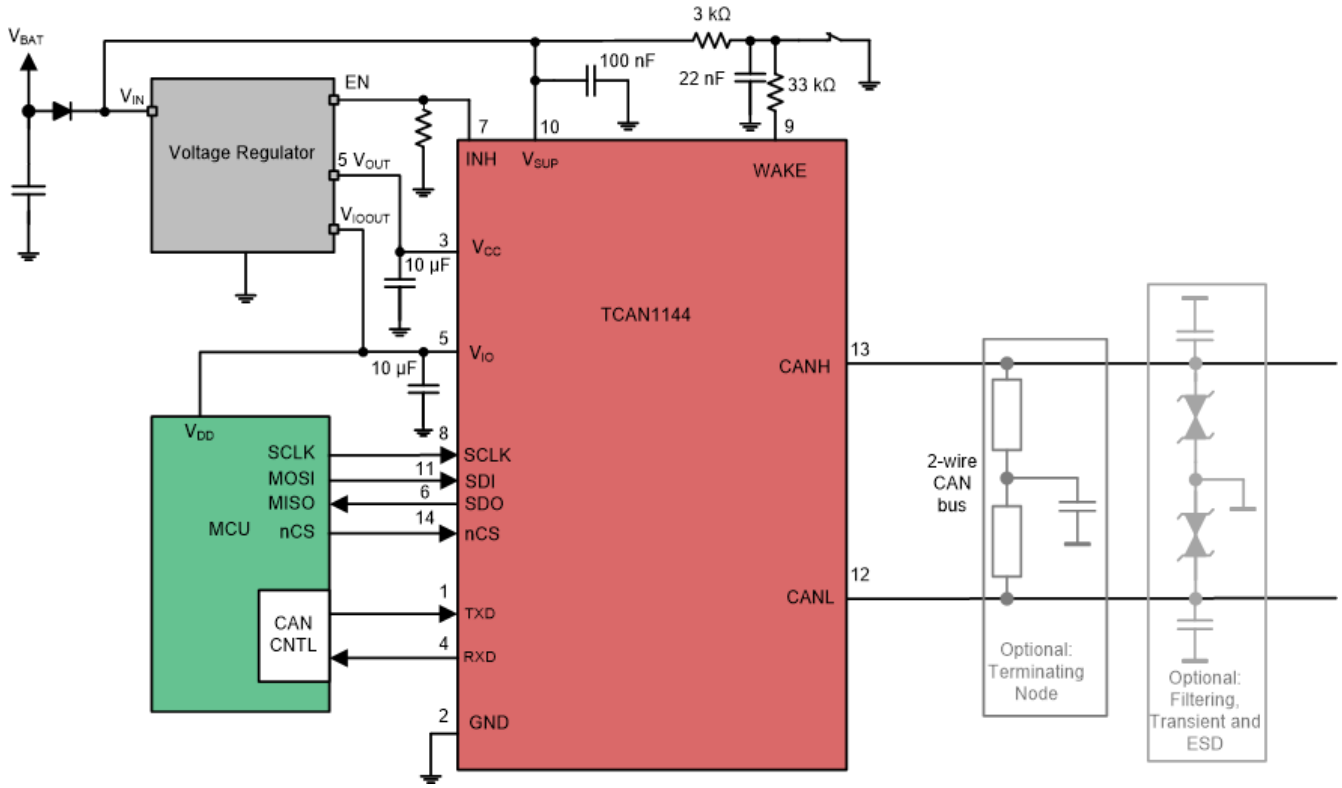


Figure 11-6. Typical CAN Applications for TCAN114x-Q1

Note: Add decoupling capacitors as needed.

11.2.1 Design Requirements

The ISO 11898-2:2016 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN114x-Q1. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2016. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. The TCAN114x-Q1 is specified to meet the 1.5 V requirement with a 50 Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TCAN114x-Q1 is a minimum of 30 kΩ. If 100 the TCAN114x-Q1 are in parallel on a bus, this is equivalent to a 300 Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60 Ω gives an equivalent loading of 50 Ω. Therefore, the TCAN114x-Q1 theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898-2:2016 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2:2016 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

11.2.2 Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination may be a single 120 Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

11.2.2.1 Brownout

Figure 11-7 shows the behavior of the INH pin during a brownout event. Brownout is when V_{SUP} is ≤ UV_{SUP} but > POR state. The RXD pin has an internal pull-up resister that is active during this event and will pull up the RXD pin output to the voltage level of V_{IO}.

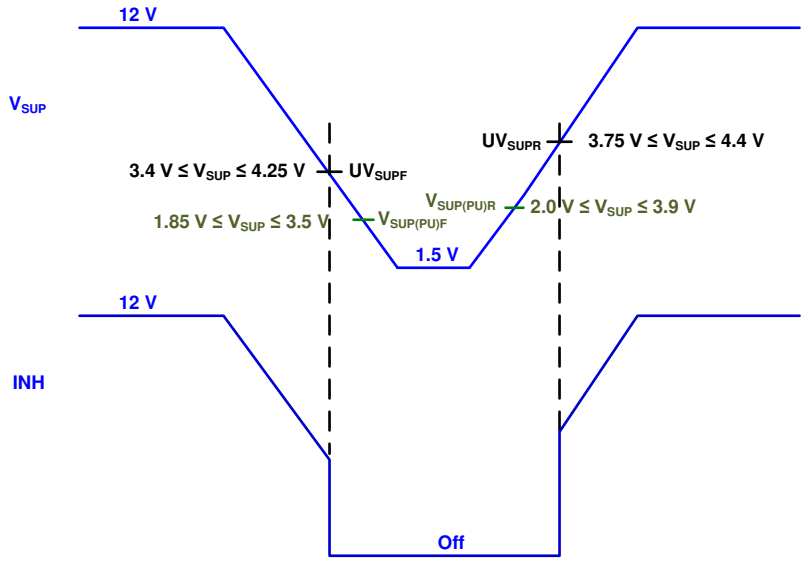
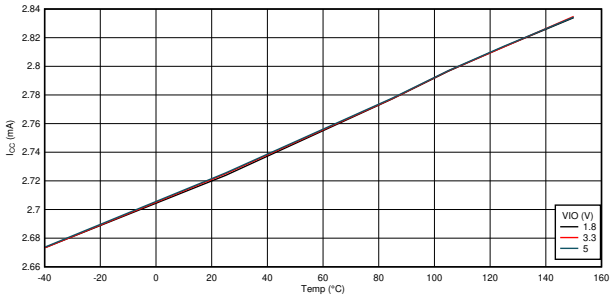


Figure 11-7. INH Behavior During Brownout

Note

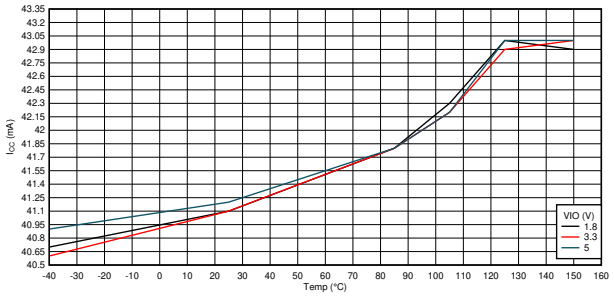
When the TCAN114x has a UV_{SUP} event, the CAN bus will be biased to ground.

11.2.3 Application Curves



V_{SUP} = 12 V V_{CC} = 5 V

Figure 11-8. Normal Mode: I_{CC} vs Temperature Recessive



V_{SUP} = 12 V V_{CC} = 5 V

Figure 11-9. Normal Mode: I_{CC} vs Temperature Dominant

12 Power Supply Recommendations

The TCAN114x-Q1 is designed to operate off of the battery Vbat and a 5 V V_{CC} supporting the CAN transceiver and low voltage CAN receiver. In order to support a wide range of microprocessors SPI is powered off of the V_{IO} pin which supports levels 1.8 V, 3.3 V and 5 V. A bulk capacitance, typically 10 µF, should be placed V_{SUP} supply with a 100 nF cap place near the V_{SUP} terminal. A bulk capacitance, typically 1 µF, should be placed near the CAN transceiver's V_{IO} supply terminal in addition to bulk capacitors near the V_{IO} source.

13 Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

13.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device itself. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C10 and C11. A series common mode choke (CMC) is placed on the CANH and CANL lines between TCAN114x-Q1 and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

A high-frequency current follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1 V_{CC} and C2 on V_{IO}, pins and C4 and C5 on the V_{SUP} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C6. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination.
- As terminal 6 (SDO/nINT) is an open drain, when working as nINT, an external resistor to V_{IO} is required. These can have a value between 2 kΩ and 10 kΩ.
- Terminal 7(INH) can have a 100 kΩ resistor to ground if not used.
- Terminal 9 (WAKE) is a bi-directional wake up that is usually connected to an external switch. It should be configured as shown with C3 which is a 22 nF capacitor to GND where R2 is 33 kΩ and R3 is 3 kΩ.
- Terminal 14 is the nCS pin.

13.2 Layout Example

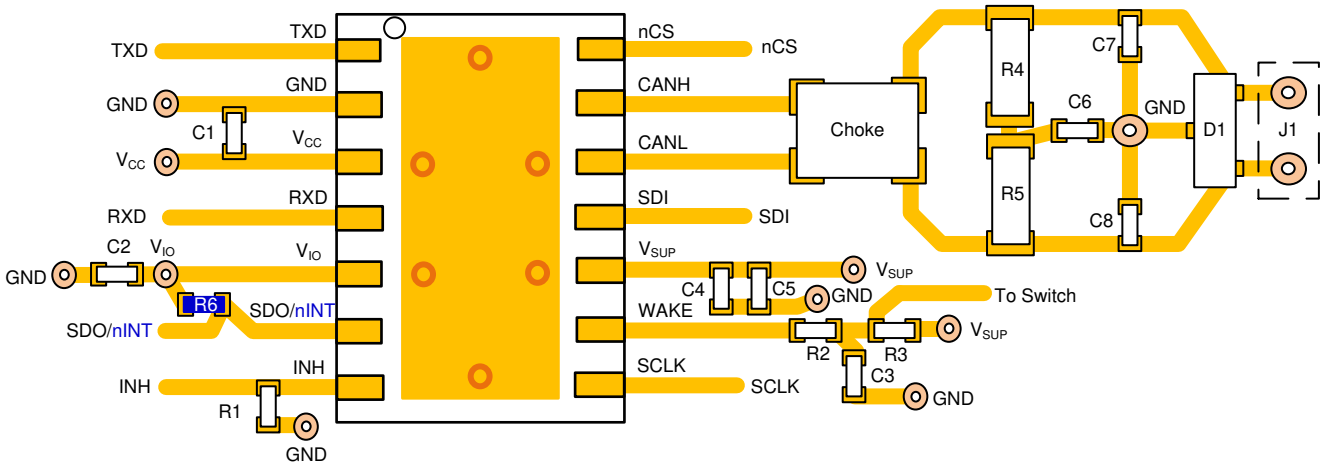


Figure 13-1. Example Layout

14 Device and Documentation Support

This device will conform to the following CAN standards. The core of what is needed is covered within this system specification, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources will be very helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

14.1 Documentation Support

14.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016: High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode)
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- GMW3122: GM requirements for HS CAN
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
- Bosch M_CAN Controller Area Network Revision 3.2.1.1 (3/24/2016)

14.1.2 EMC Requirements:

- SAE J2962-2: Communication Transceivers Qualification Requirements - CAN
- HW Requirements for CAN, LIN,FR V1.3: German OEM requirements for HS CAN

14.1.3 Conformance Test Requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

14.1.4 Related Documentation

- “A Comprehensible Guide to Controller Area Network”, Wilfried Voss, Copperhill Media Corporation
- “CAN System Engineering: From Theory to Practical Applications”, 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

14.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1144DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1144
TCAN1144DRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1144
TCAN1144DYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1144
TCAN1145DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1145
TCAN1145DRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1145
TCAN1145DYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1145
TCAN1146DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1146
TCAN1146DRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1146
TCAN1146DYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1146

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

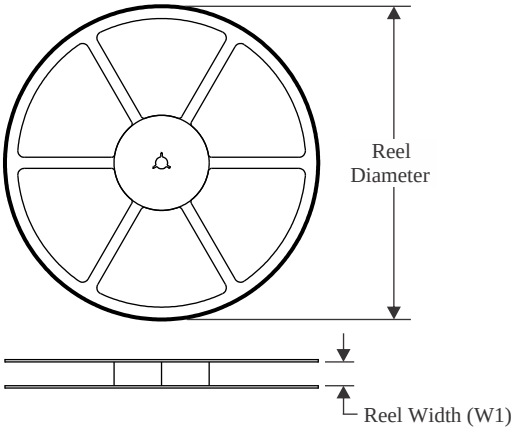
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

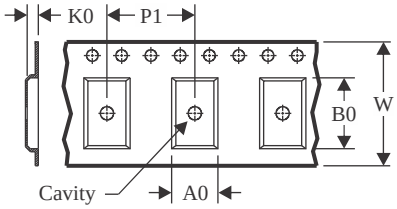
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

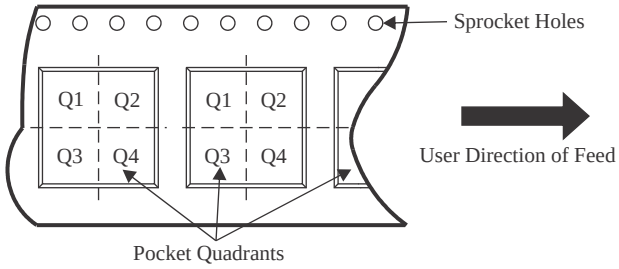


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

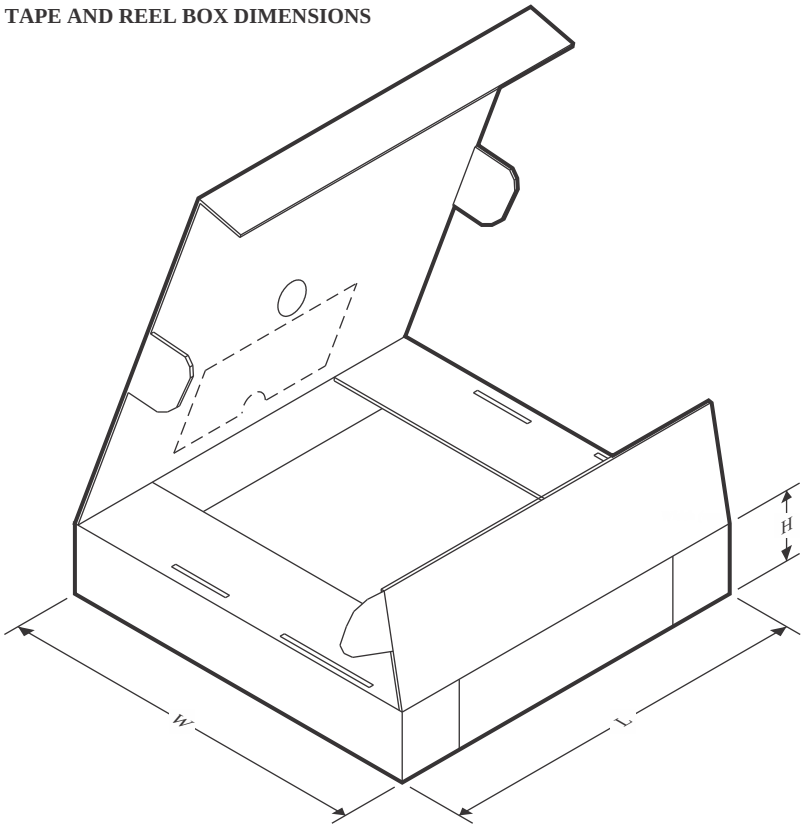
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1144DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1144DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1144DYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TCAN1145DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1145DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1145DYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TCAN1146DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1146DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1146DYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

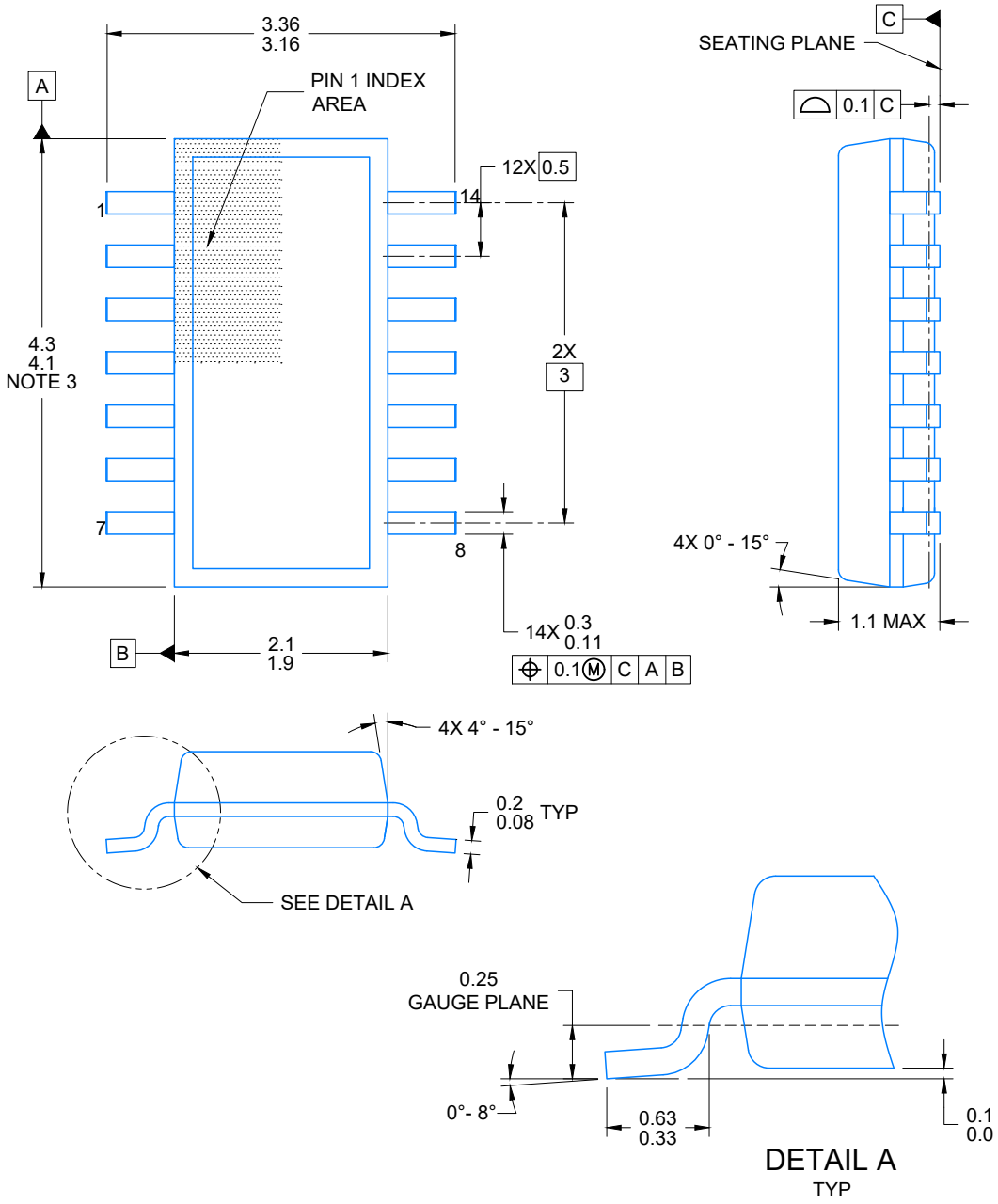
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1144DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1144DRQ1	SOIC	D	14	2500	367.0	367.0	38.0
TCAN1144DYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TCAN1145DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1145DRQ1	SOIC	D	14	2500	367.0	367.0	38.0
TCAN1145DYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TCAN1146DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1146DRQ1	SOIC	D	14	2500	367.0	367.0	38.0
TCAN1146DYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

PACKAGE OUTLINE

DYY0014A

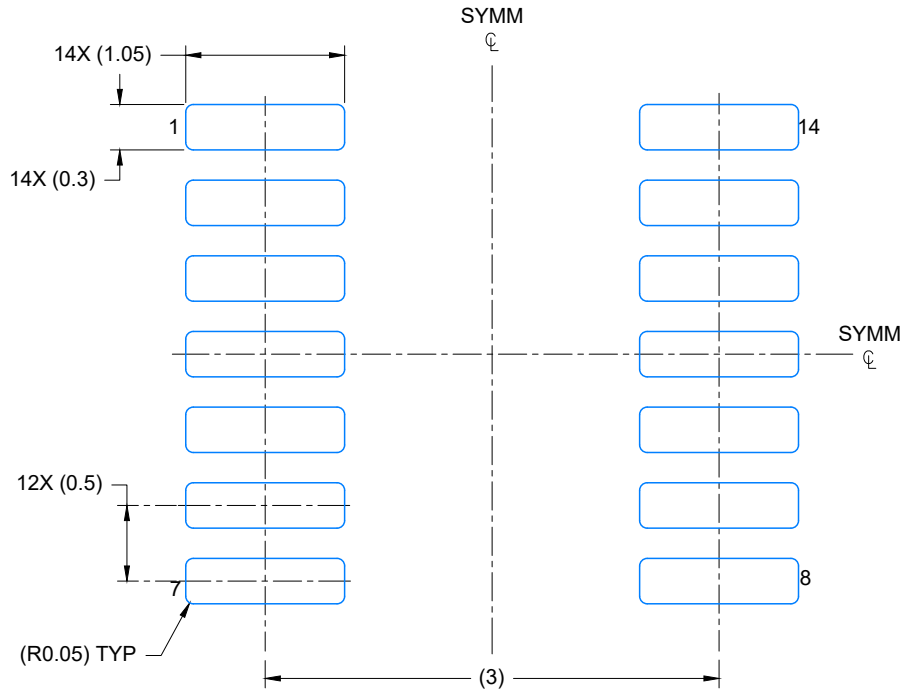
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

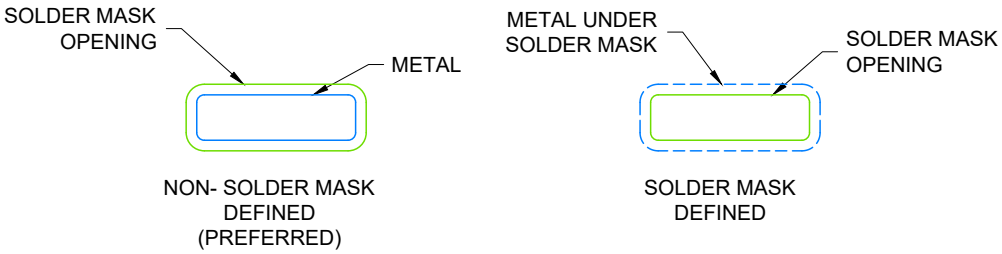


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

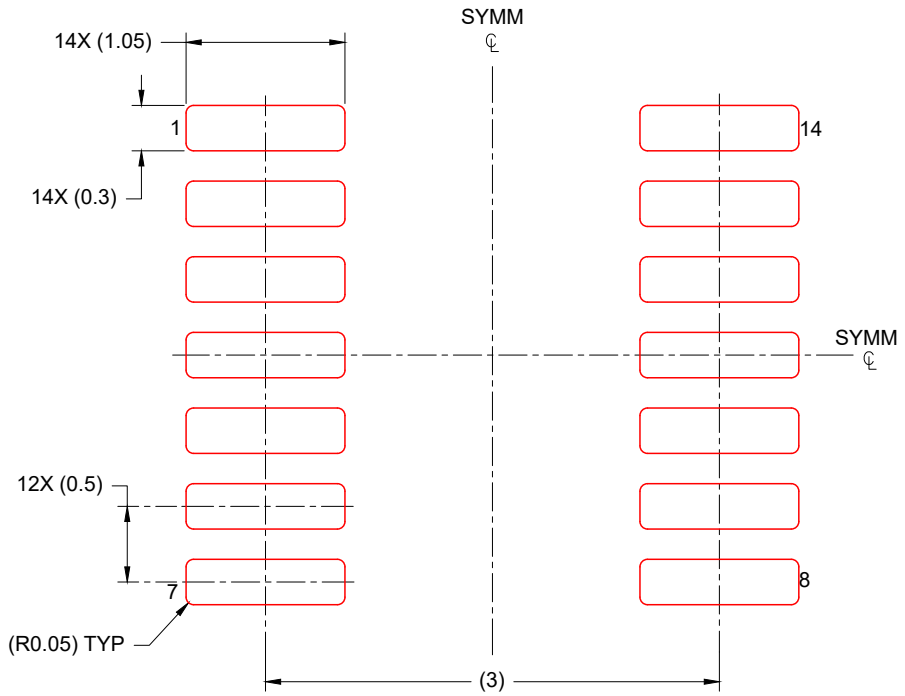


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

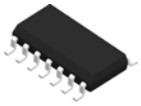


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

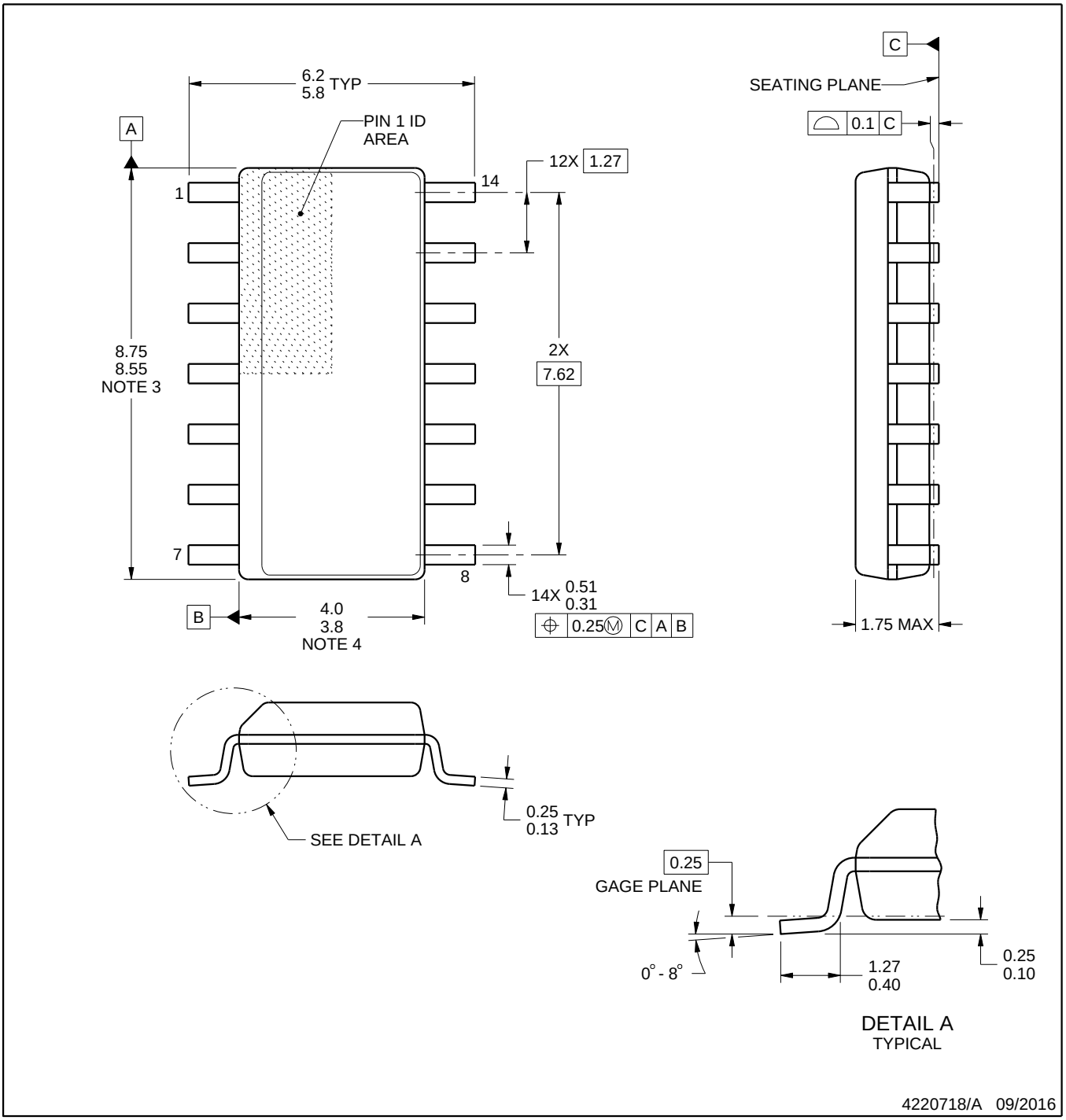


PACKAGE OUTLINE

D0014A

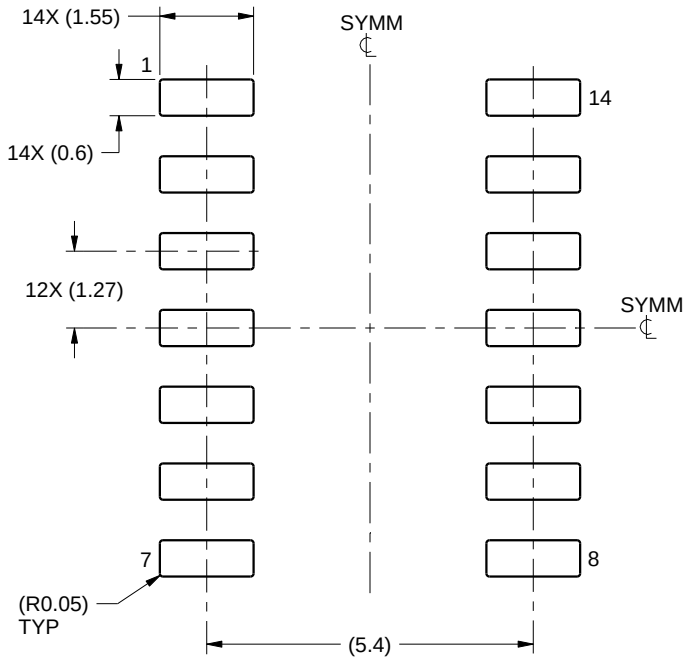
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

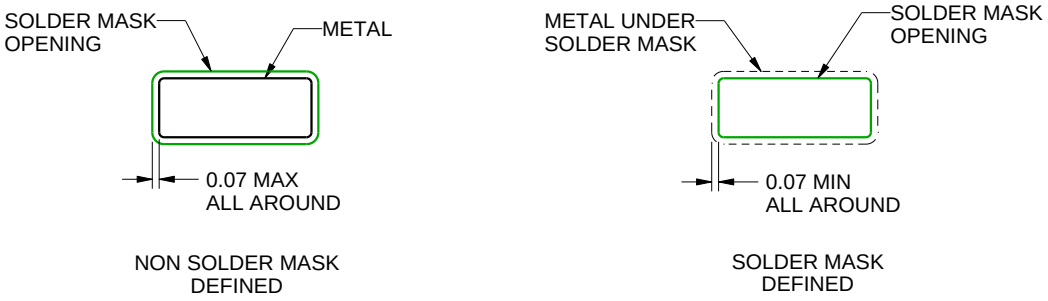


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

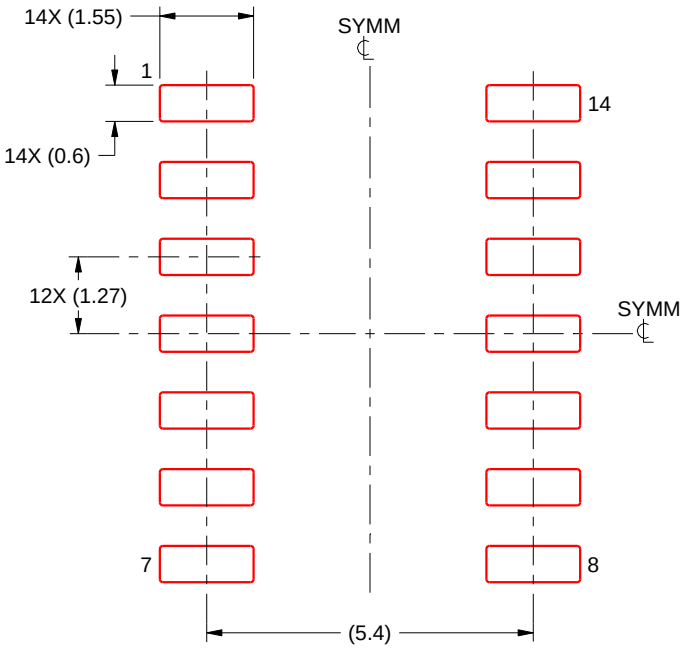
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

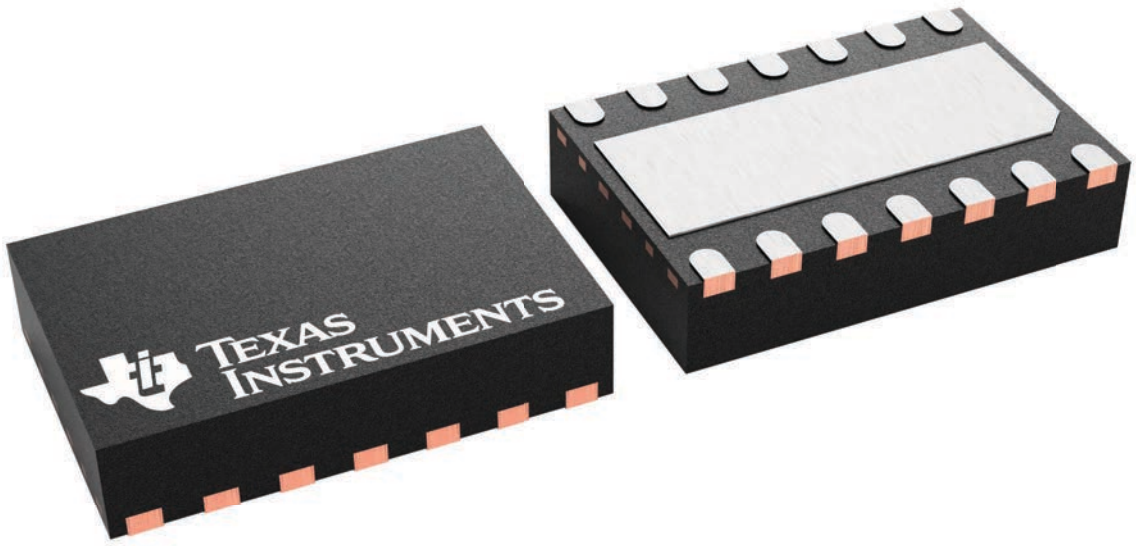
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



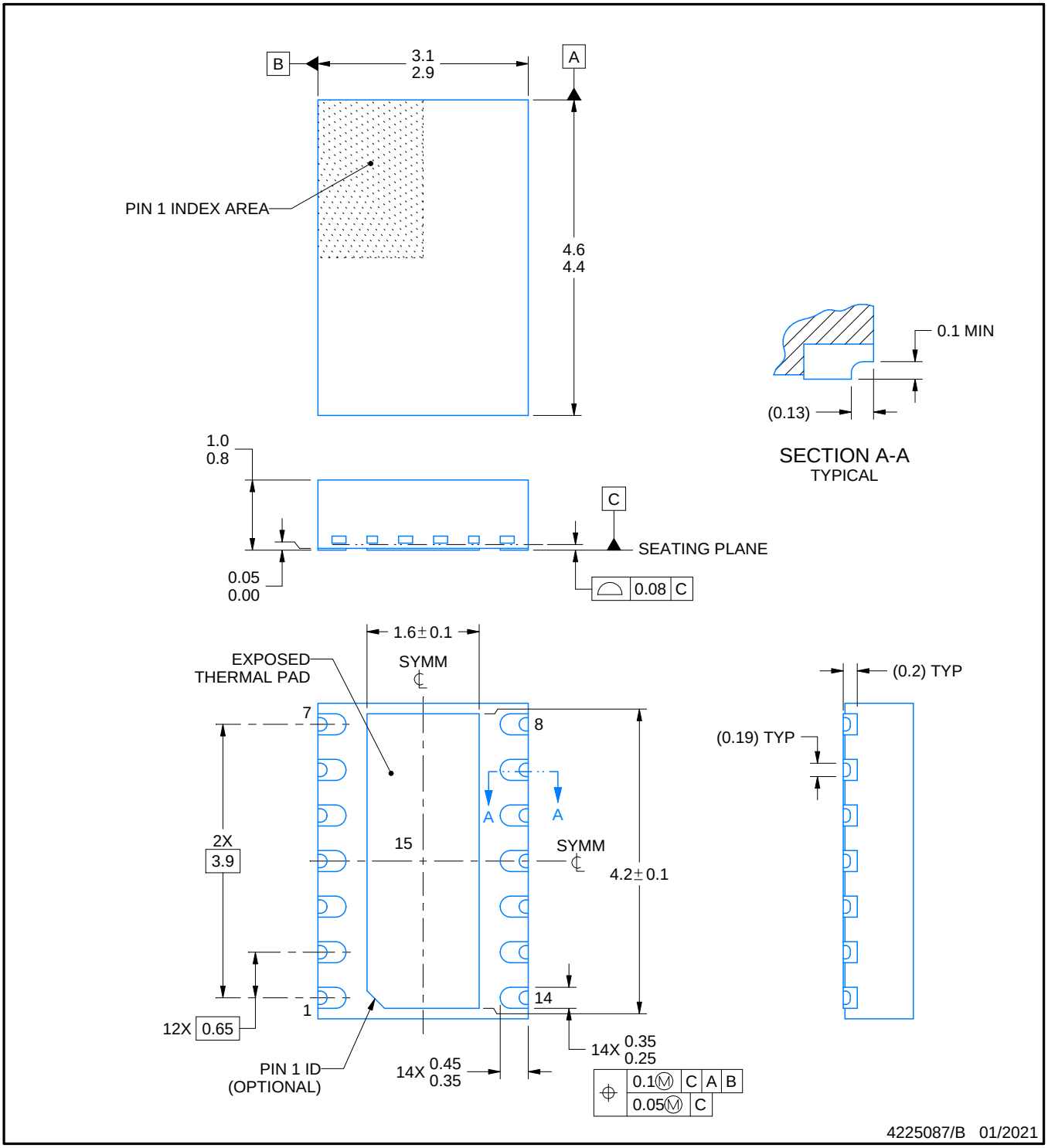
4225088/A

DMT0014B

PACKAGE OUTLINE

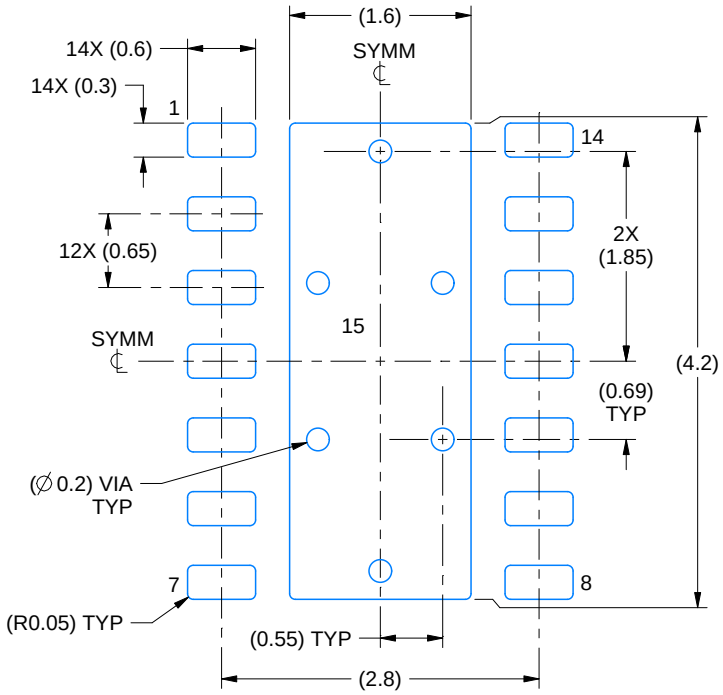
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

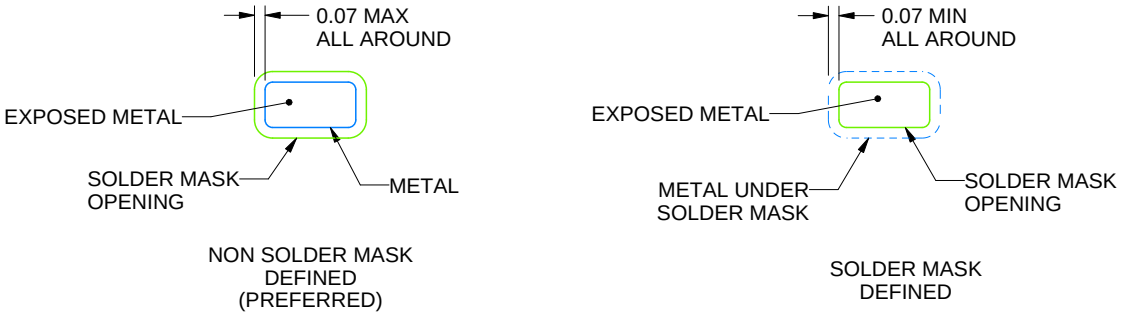


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

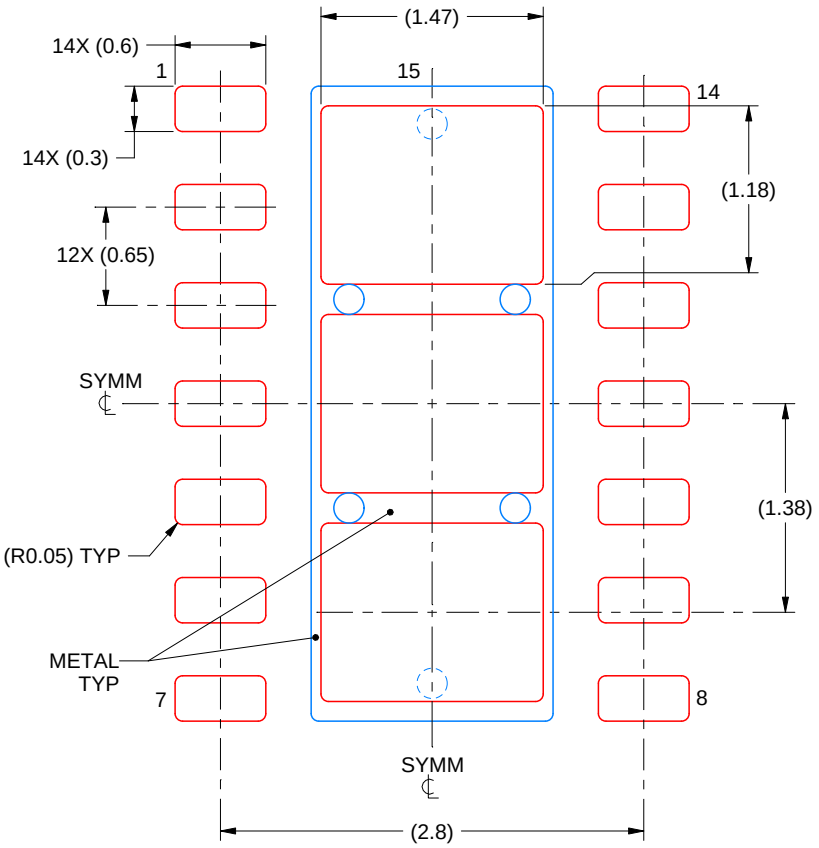


SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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