

S9KEA128P80M48SF0

KEA128 Sub-Family Data Sheet Supports the following: S9KEAZ64AMLK(R), S9KEAZ128AMLK(R), S9KEAZ64AVLK(R), S9KEAZ128AVLK(R), S9KEAZ64ACLK(R), S9KEAZ128ACLK(R), S9KEAZ64AMLH(R), S9KEAZ128AMLH(R), S9KEAZ64AVLH(R), S9KEAZ128AVLH(R), S9KEAZ64ACLH(R) and S9KEAZ128ACLH(R)

Rev. 6 — 30 January 2024

Data sheet

1 Key features

1.1 Operating characteristics

- Voltage range: 2.7 to 5.5 V
- Flash write voltage range: 2.7 to 5.5 V
- Temperature range (ambient): -40 to 125°C

1.2 Performance

- Up to 48 MHz Arm® Cortex-M0+ core
- Single cycle 32-bit x 32-bit multiplier
- Single cycle I/O access port

1.3 Memories and memory interfaces

- Up to 128 KB flash
- Up to 16 KB RAM

1.4 Clocks

- Oscillator (OSC) - supports 32.768 kHz crystal or 4 MHz to 24 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
- Internal clock source (ICS) - internal FLL with internal or external reference, 37.5 kHz pre-trimmed internal reference for 48 MHz system clock
- Internal 1 kHz low-power oscillator (LPO)

1.5 System peripherals

- Power management module (PMC) with three power modes: Run, Wait, Stop
- Low-voltage detection (LVD) with reset or interrupt, selectable trip points
- Watchdog with independent clock source (WDOG)
- Programmable cyclic redundancy check module (CRC)
- Serial wire debug interface (SWD)
- Aliased SRAM bitband region (BIT-BAND)
- Bit manipulation engine (BME)



1.6 Security and integrity modules

- 80-bit unique identification (ID) number per chip

1.7 Human-machine interface

- Up to 71 general-purpose input/output (GPIO)
- Two 32-bit keyboard interrupt modules (KBI)
- External interrupt (IRQ)

1.8 Analog modules

- One up to 16-channel 12-bit SAR ADC, operation in Stop mode, optional hardware trigger (ADC)
- Two analog comparators containing a 6-bit DAC and programmable reference input (ACMP)

1.9 Timers

- One 6-channel FlexTimer/PWM (FTM)
- Two 2-channel FlexTimer/PWM (FTM)
- One 2-channel periodic interrupt timer (PIT)
- One pulse width timer (PWT)
- One real-time clock (RTC)

1.10 Communication interfaces

- Two SPI modules (SPI)
- Up to three UART modules (UART)
- Two I2C modules (I2C)
- One MSCAN module (MSCAN)

1.11 Package options

- 80-pin LQFP
- 64-pin LQFP

2 Ordering parts

2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: KEAZ128 .

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

Q B KEA A C FFF M T PP N

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> S = Automotive qualified P = Prequalification
B	Memory type	<ul style="list-style-type: none"> 9 = Flash
KEA	Kinetis Auto family	<ul style="list-style-type: none"> KEA
A	Key attribute	<ul style="list-style-type: none"> Z = M0+ core F = M4 W/ DSP & FPU C = M4 W/ AP + FPU
C	CAN availability	<ul style="list-style-type: none"> N = CAN not available (Blank) = CAN available
FFF	Program flash memory size	<ul style="list-style-type: none"> 128 = 128 KB
M	Maskset identifier	<ul style="list-style-type: none"> A = TSMC10 Mask Rev2 W0 = TSMC11 Mask Rev0 B = TSMC10 Mask Rev2 or TSMC11 Mask Rev0
T	Temperature range (°C)	<ul style="list-style-type: none"> C = -40 to 85 V = -40 to 105 M = -40 to 125
PP	Package identifier	<ul style="list-style-type: none"> LH = 64 LQFP (10 mm x 10 mm) LK = 80 LQFP (14 mm x 14 mm)
N	Packaging type	<ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays

3.4 Example

This is an example part number:

S9KEAZ128AMLK

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	[1]
T _{SDR}	Solder temperature, lead-free	—	260	°C	[2]

[1] Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

[2] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	[1]

[1] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	−6000	+6000	V	[1]
V _{CDM}	Electrostatic discharge voltage, charged-device model	−500	+500	V	[2]
I _{LAT}	Latch-up current at ambient temperature of °C	−100	+100	mA	[3]

[1] Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

[2] Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

[3] Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*. The test produced the following results:

- Test was performed at 125 °C case temperature (Class II).
- I/O pins pass +100/-100 mA I-test with I_{DD} current limit at 400 mA (V_{DD} collapsed during positive injection).
- I/O pins pass +50/-100 mA I-test with I_{DD} current limit at 1000 mA for V_{DD}.
- Supply groups pass 1.5 V_{ccmax}.
- RESET_B pin was only tested with negative I-test due to product conditioning requirement.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 1. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	−0.3	6.0	V
I _{DD}	Maximum current into V _{DD}	—	120	mA
V _{IN}	Input voltage except true open drain pins	−0.3	V _{DD} + 0.3 ^[1]	V
	Input voltage of true open drain pins	−0.3	6	V
I _D	Instantaneous maximum current single pin limit (applies to all port pins)	−25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} − 0.3	V _{DD} + 0.3	V

[1] Maximum rating of V_{DD} also applies to V_{IN}.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	Descriptions		Min	Typical ^[1]	Max	Unit
—	Operating voltage		—	2.7	—	5.5 V
T _{ramp} ^[2]	MCU supply ramp rate		85°C	—	—	85 V/ms
			105°C	—	—	70
			125°C	—	—	60
V _{OH}	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, I _{load} = -5 mA	V _{DD} - 0.8	—	— V
			3 V, I _{load} = -2.5 mA	V _{DD} - 0.8	—	— V
	High current drive pins, high-drive strength ^[3]		5 V, I _{load} = -20 mA	V _{DD} - 0.8	—	— V
			3 V, I _{load} = -10 mA	V _{DD} - 0.8	—	— V
I _{OHT}	Output high current	Max total I _{OH} for all ports	5 V	—	—	-100 mA
			3 V	—	—	-60
V _{OL}	Output low voltage	All I/O pins, standard-drive strength	5 V, I _{load} = 5 mA	—	—	0.8 V
			3 V, I _{load} = 2.5 mA	—	—	0.8 V
	High current drive pins, high-drive strength ^[3]		5 V, I _{load} = 20 mA	—	—	0.8 V
			3 V, I _{load} = 10 mA	—	—	0.8 V
I _{OLT}	Output low current	Max total I _{OL} for all ports	5 V	—	—	100 mA
			3 V	—	—	60
V _{IH}	Input high voltage	All digital inputs	4.5 ≤ V _{DD} < 5.5 V	0.65 × V _{DD}	—	— V
			2.7 ≤ V _{DD} < 4.5 V	0.70 × V _{DD}	—	—
V _{IL}	Input low voltage	All digital inputs	4.5 ≤ V _{DD} < 5.5 V	—	—	0.35 × V _{DD}
			2.7 ≤ V _{DD} < 4.5 V	—	—	0.30 × V _{DD}
V _{hys}	Input hysteresis	All digital inputs	—	0.06 × V _{DD}	—	mV
I _{in}	Input leakage current	Per pin (pins in high impedance input mode)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1 μA
I _{INTOT}	Total leakage combined for all port pins	Pins in high impedance input mode	V _{IN} = V _{DD} or V _{SS}	—	—	2 μA

Table 2. DC characteristics...continued

Symbol	Descriptions		Min	Typical ^[1]	Max	Unit
R _{PU}	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	—	50.0	kΩ
R _{PU} ^[4]	Pullup resistors	PTA2 and PTA3 pins	—	—	60.0	kΩ
I _{IC}	DC injection current ^{[5][6][7]}	Single pin limit	V _{IN} < V _{SS} , V _{IN} > V _{DD}	—	2	mA
		Total MCU limit, includes sum of all stressed pins		-5	25	
C _{In}	Input capacitance, all pins		—	—	7	pF
V _{RAM}	RAM retention voltage		—	—	—	V

- [1] Typical values are measured at 25 °C. Characterized, not tested.
- [2] Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
- [3] Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.
- [4] The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- [5] All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
- [6] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
- [7] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current (V_{in} > V_{DD}) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR specification

Symbol	Description		Min	Typ	Max	Unit
V _{POR}	POR re-arm voltage ^[1]		1.5	1.75	2.0	V
V _{LVDH}	Falling low-voltage detect threshold—high range (LVDV = 1) ^[2]		4.2	4.3	4.4	V
V _{LW1H}	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LW2H}		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LW3H}		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LW4H}		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LW1L}	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LW2L}		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V

Table 3. LVD and POR specification...continued

Symbol	Description	Min	Typ	Max	Unit
V_{LVW3L}	Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}		2.92	3.0	3.08	V
V_{HYSDL}	Low range low-voltage detect hysteresis	—	40	—	mV
V_{HYSWL}	Low range low-voltage warning hysteresis	—	80	—	mV
V_{BG}	Buffered bandgap output ^[3]	1.14	1.16	1.18	V

- [1] Maximum is highest voltage that POR is guaranteed.
- [2] Rising thresholds are falling threshold + hysteresis.
- [3] voltage Factory trimmed at $V_{DD} = 5.0$ V, Temp = 125 °C

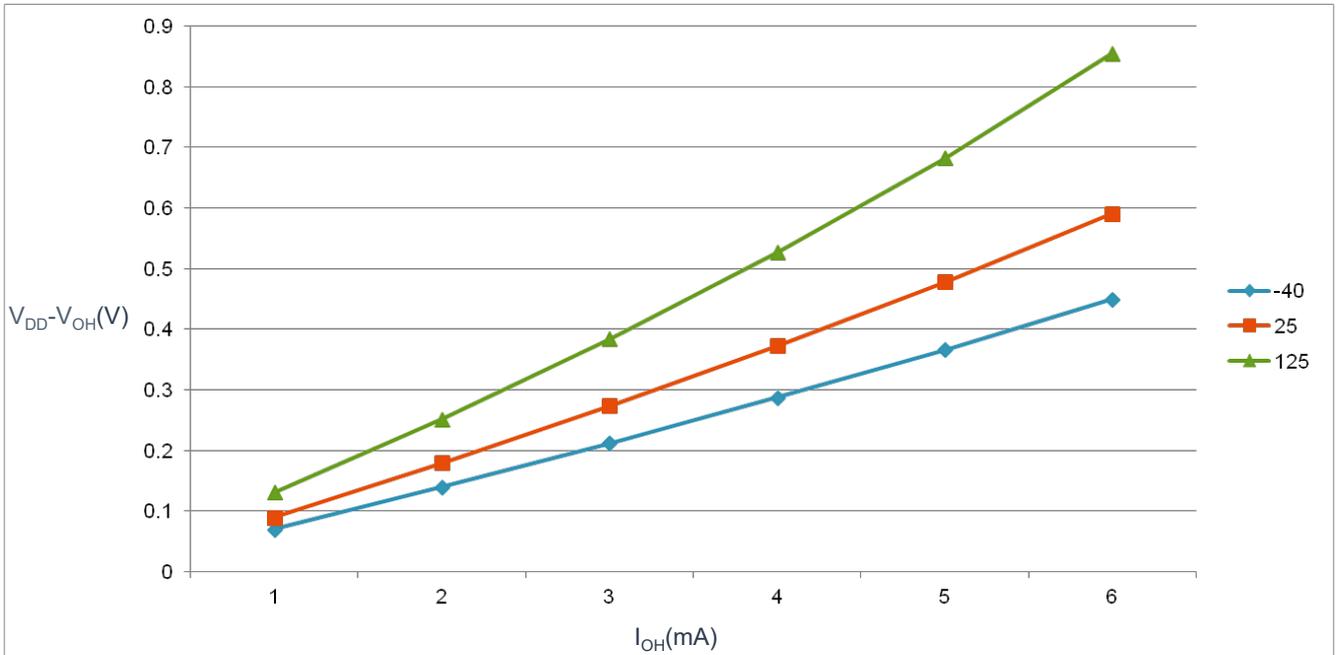


Figure 1. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (standard drive strength) ($V_{DD} = 5$ V)

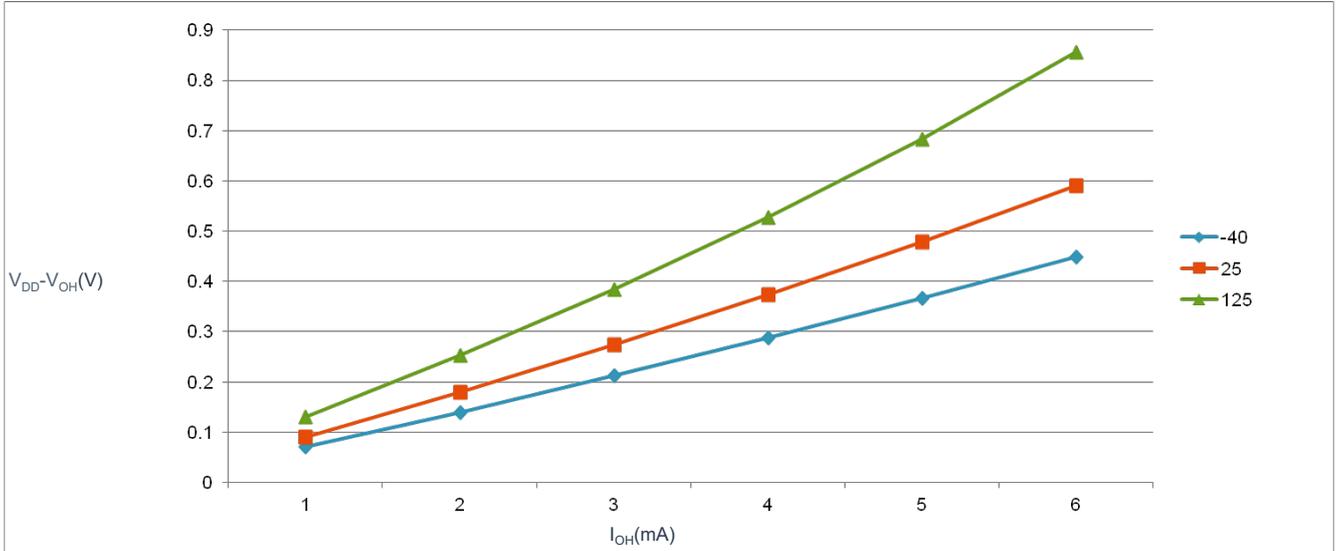


Figure 2. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (standard drive strength) ($V_{DD} = 3\text{ V}$)

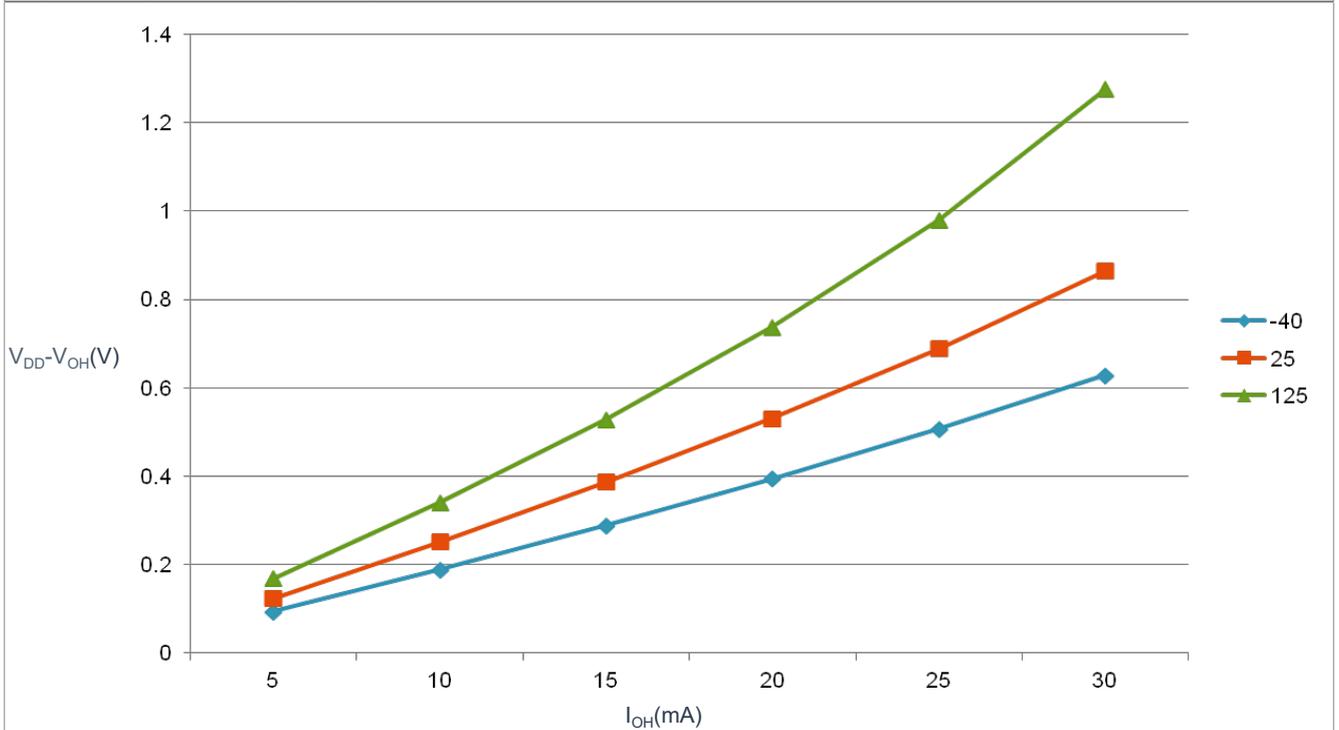


Figure 3. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (high drive strength) ($V_{DD} = 5\text{ V}$)

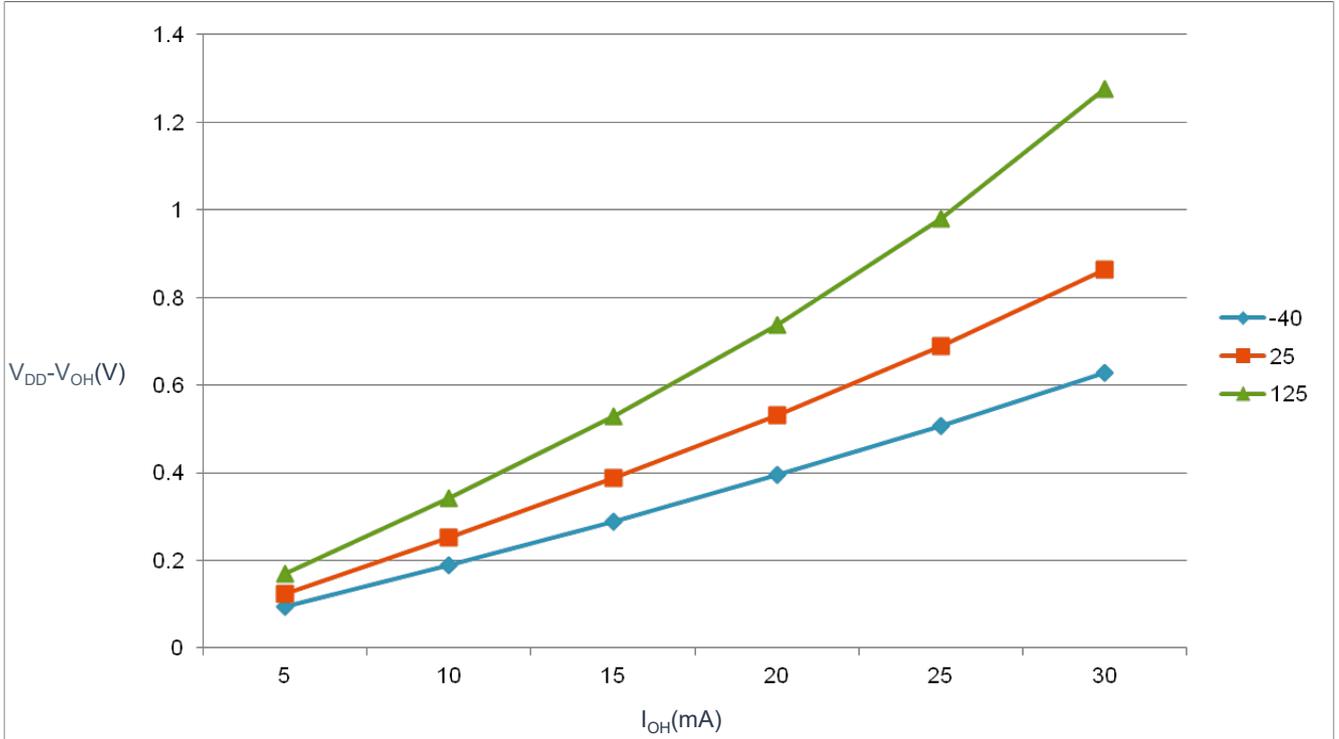


Figure 4. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (high drive strength) ($V_{DD} = 3\text{ V}$)

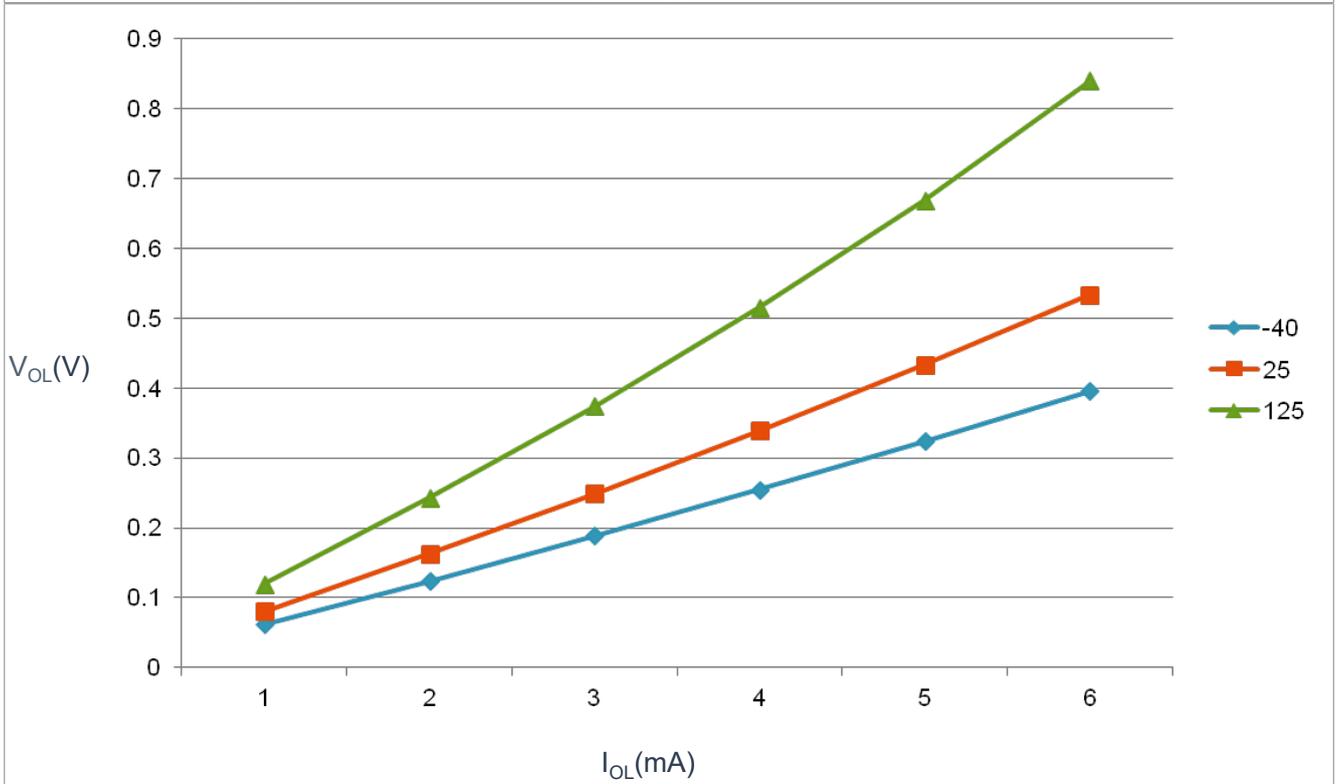


Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) ($V_{DD} = 5\text{ V}$)

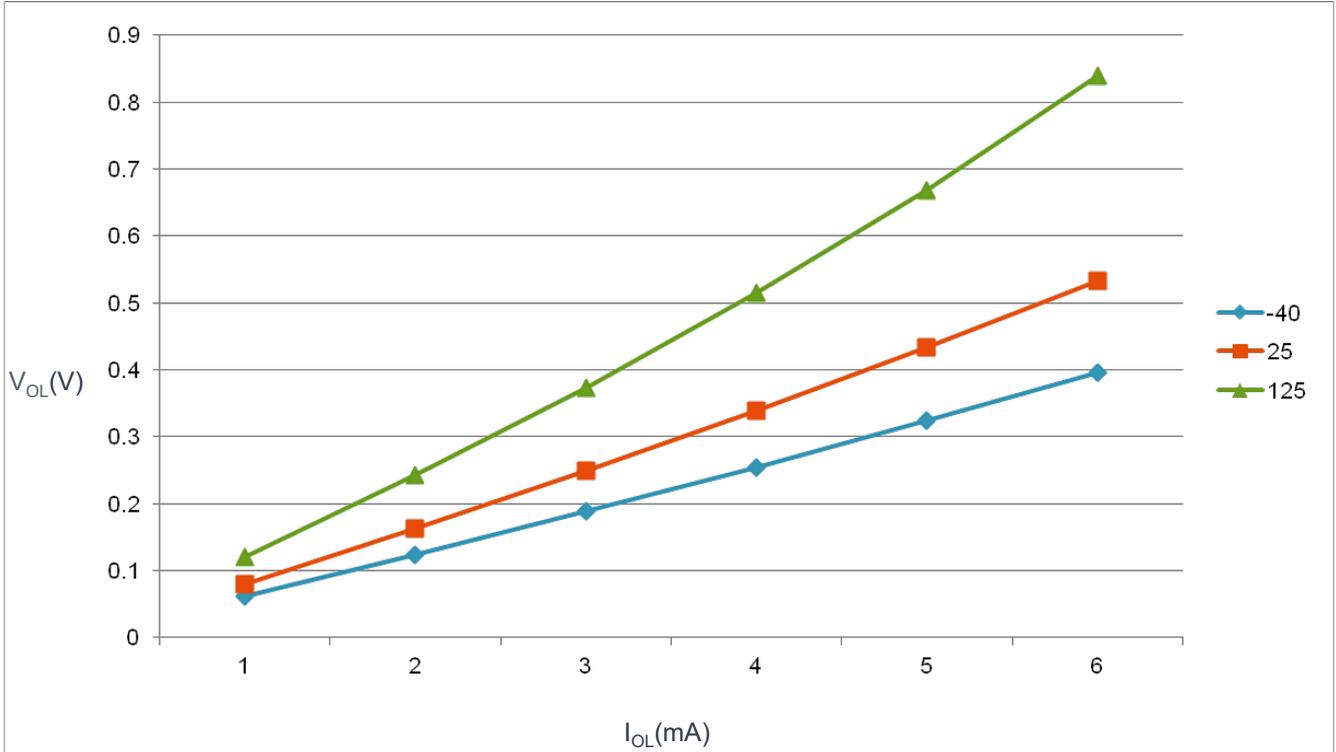


Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) ($V_{DD} = 3\text{ V}$)

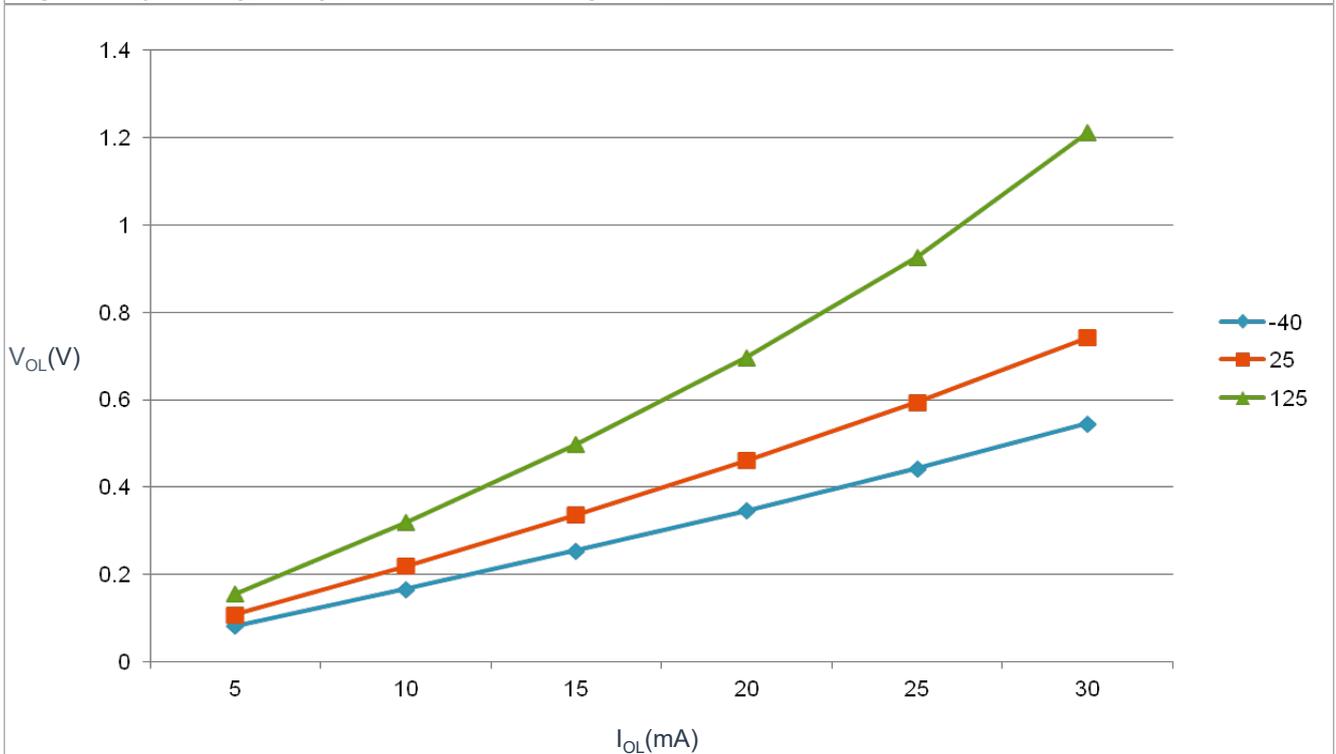


Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

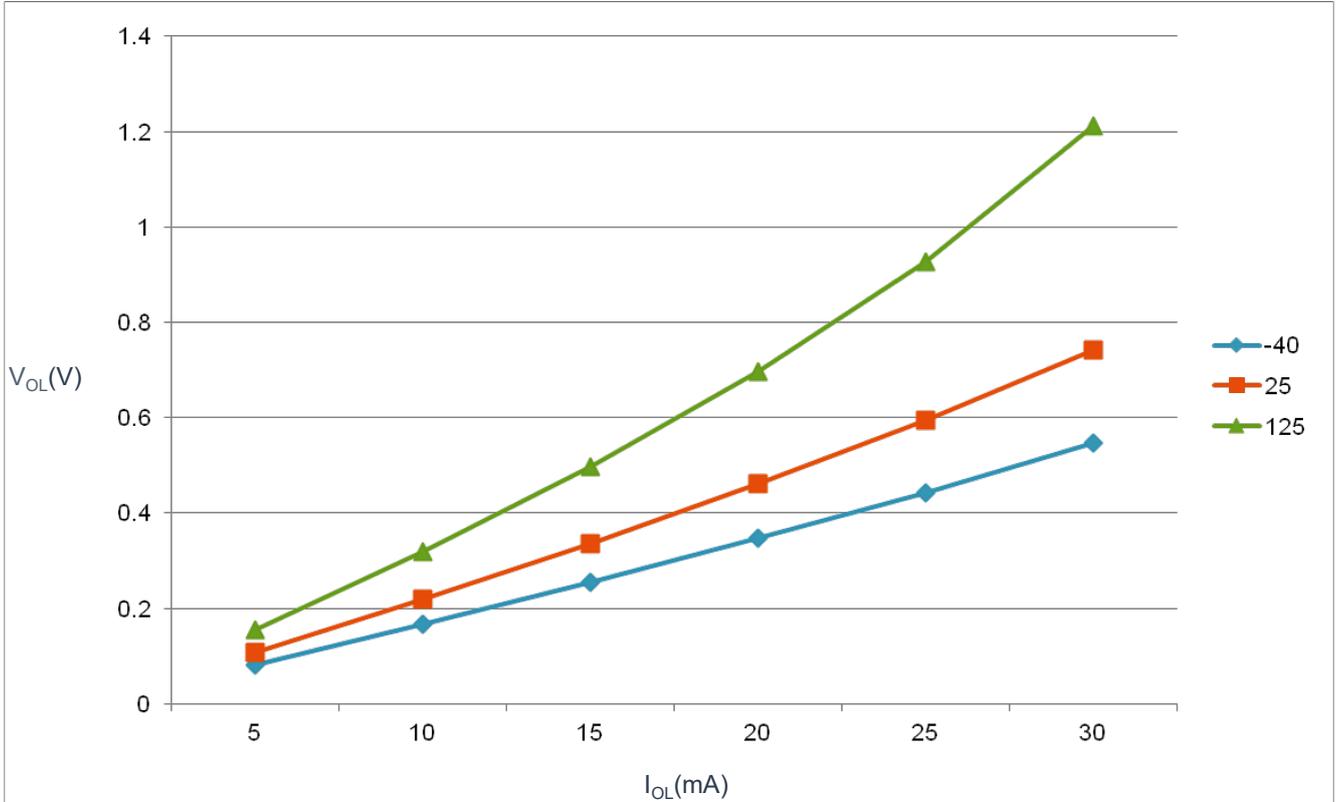


Figure 8. Typical VOL Vs. IOL (high drive strength) (VDD = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Parameter	Symbol	Core/Bus Freq	VDD (V)	Typical ^[1]	Max	Unit	Temp
Run supply current FEI mode, all modules clocks enabled; run from flash	RI _{DD}	48/24 MHz	5	11.1	—	mA	-40 to 125 °C
		24/24 MHz		8	—		
		12/12 MHz		5	—		
		1/1 MHz		2.4	—		
		48/24 MHz	3	11	—		
		24/24 MHz		7.9	—		
		12/12 MHz		4.9	—		
		1/1 MHz		2.3	—		
Run supply current FEI mode, all modules clocks disabled and gated; run from flash	RI _{DD}	48/24 MHz	5	7.8	—	mA	-40 to 125 °C
		24/24 MHz		5.5	—		
		12/12 MHz		3.8	—		
		1/1 MHz		2.3	—		
		48/24 MHz	3	7.7	—		

Table 4. Supply current characteristics...continued

Parameter	Symbol	Core/Bus Freq	V _{DD} (V)	Typical ^[1]	Max	Unit	Temp
		24/24 MHz		5.4	—		
		12/12 MHz		3.7	—		
		1/1 MHz		2.2	—		
Run supply current FBE mode, all modules clocks enabled; run from RAM	R _I DD	48/24 MHz	5	14.7	—	mA	-40 to 125 °C
		24/24 MHz		9.8	14.9 ^[2]		
		12/12 MHz		6	—		
		1/1 MHz		2.4	—		
		48/24 MHz	3	14.6	—		
		24/24 MHz		9.6	12.8 ^[2]		
		12/12 MHz		5.9	—		
		1/1 MHz		2.3	—		
Run supply current FBE mode, all modules clocks disabled and gated; run from RAM	R _I DD	48/24 MHz	5	11.4	—	mA	-40 to 125 °C
		24/24 MHz		7.7	12.5 ^[2]		
		12/12 MHz		4.7	—		
		1/1 MHz		2.3	—		
		48/24 MHz	3	11.3	—		
		24/24 MHz		7.6	9.5 ^[2]		
		12/12 MHz		4.6	—		
		1/1 MHz		2.2	—		
Wait mode current FEI mode, all modules clocks enabled	W _I DD	48/24 MHz	5	8.4	—	mA	-40 to 125 °C
		24/24 MHz		6.5	7.2 ^[2]		
		12/12 MHz		4.3	—		
		1/1 MHz		2.4	—		
		48/24 MHz	3	8.3	—		
		24/24 MHz		6.4	7.1 ^[2]		
		12/12 MHz		4.2	—		
		1/1 MHz		2.3	—		
Stop mode supply current no clocks active (except 1 kHz LPO clock) ^[3]	S _I DD	—	5	2	170 ^[2]	μA	-40 to 125 °C
		—	3	1.9	160 ^[2]		-40 to 125 °C
ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	86	—	μA	-40 to 125 °C
			3	82	—		
ACMP adder to Stop	—	—	5	12	—	μA	-40 to 125 °C

Table 4. Supply current characteristics...continued

Parameter	Symbol	Core/Bus Freq	V _{DD} (V)	Typical ^[1]	Max	Unit	Temp
			3	12	—		
LVD adder to Stop ^[4]	—	—	5	130	—	μA	-40 to 125 °C
			3	125	—		

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
 [2] The high current is observed at high temperature.
 [3] RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
 [4] LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following NXP applications notes, available on nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

Num	Rating	Symbol	Min	Typical ^[1]	Max	Unit
1	System and core clock	f _{Sys}	DC	—	48	MHz
2	Bus frequency (t _{cyc} = 1/f _{Bus})	f _{Bus}	DC	—	24	MHz
3	Internal low power oscillator frequency	f _{LPO}	0.67	1.0	1.25	KHz
4	External reset pulse width ^[2]	t _{extrst}	1.5 × t _{cyc}	—	—	ns
5	Reset low drive	t _{rstdrv}	34 × t _{cyc}	—	—	ns
6	IRQ pulse width	Asynchronous path ^[2]	t _{LIH}	100	—	ns
		Synchronous path ^[3]	t _{HIL}	1.5 × t _{cyc}	—	ns
7	Keyboard interrupt pulse width	Asynchronous path ^[2]	t _{LIH}	100	—	ns
		Synchronous path	t _{HIL}	1.5 × t _{cyc}	—	ns
8	Port rise and fall time - Normal drive strength (load = 50 pF) ^[4]	—	t _{Rise}	—	10.2	ns
		—	t _{Fall}	—	9.5	ns

Table 5. Control timing...continued

Num	Rating	Symbol	Min	Typical ^[1]	Max	Unit
	Port rise and fall time - high drive strength (load = 50 pF) ^[4]	t_{Rise}	—	5.4	—	ns
		t_{Fall}	—	4.6	—	ns

- [1] Typical values are based on characterization data at $V_{DD} = 5.0\text{ V}$, $25\text{ }^\circ\text{C}$ unless otherwise stated.
- [2] This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
- [3] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
- [4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$.

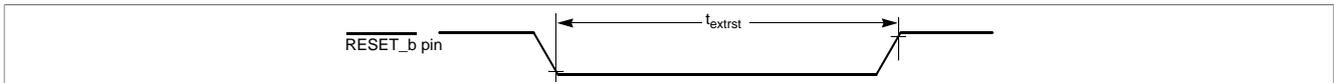


Figure 9. Reset timing

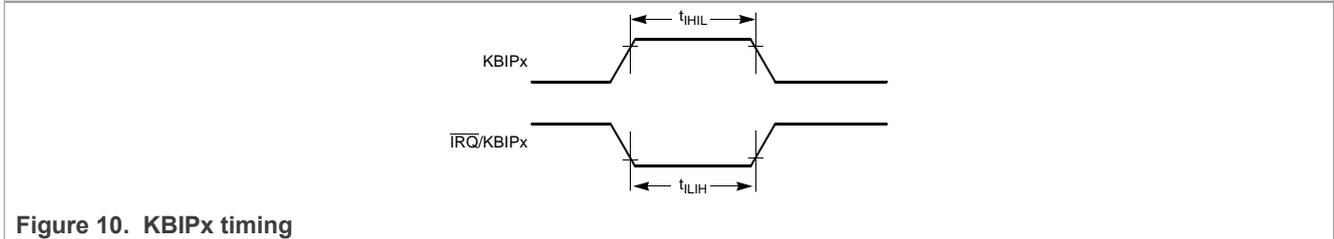


Figure 10. KBIPx timing

5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 6. FTM input timing

Function	Symbol	Min	Max	Unit
Timer clock frequency	f_{Timer}	f_{Bus}	f_{Sys}	Hz
External clock frequency	f_{TCLK}	0	$f_{Timer}/4$	Hz
External clock period	t_{TCLK}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{CPW}	1.5	—	t_{cyc}

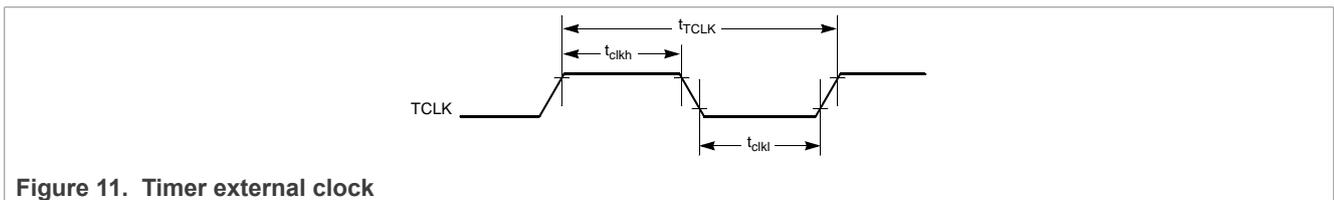
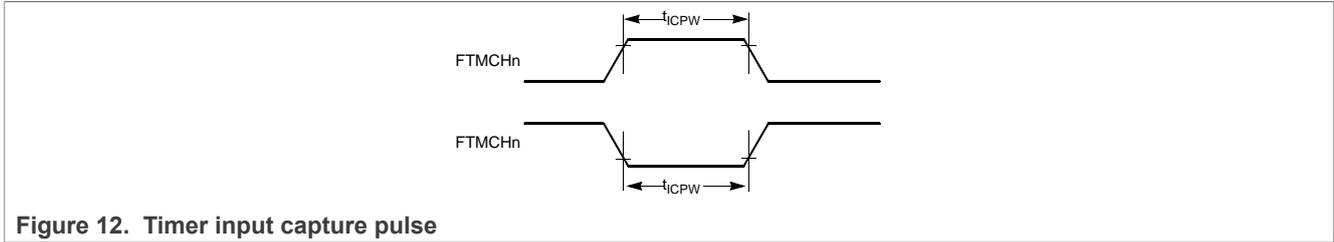


Figure 11. Timer external clock



5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal attributes

Board type	Symbol	Description	64 LQFP	80 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	57	°C/W	[1], [2]
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	44	°C/W	[1], [3]
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	47	°C/W	[1], [3]
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	38	°C/W	[1], [3]
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	28	°C/W	[4]
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	15	°C/W	[5]
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	3	°C/W	[6]

- [1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- [2] Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
- [3] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- [4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- [5] Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
- [6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$$P_D = P_{int} + P_{I/O}$$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ }^\circ\text{C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ }^\circ\text{C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A .

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 8. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

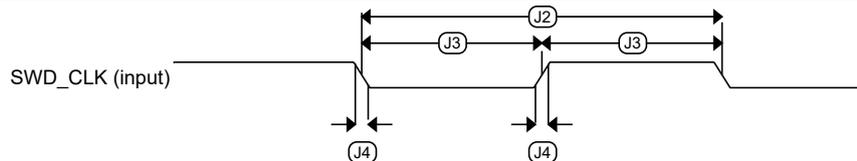
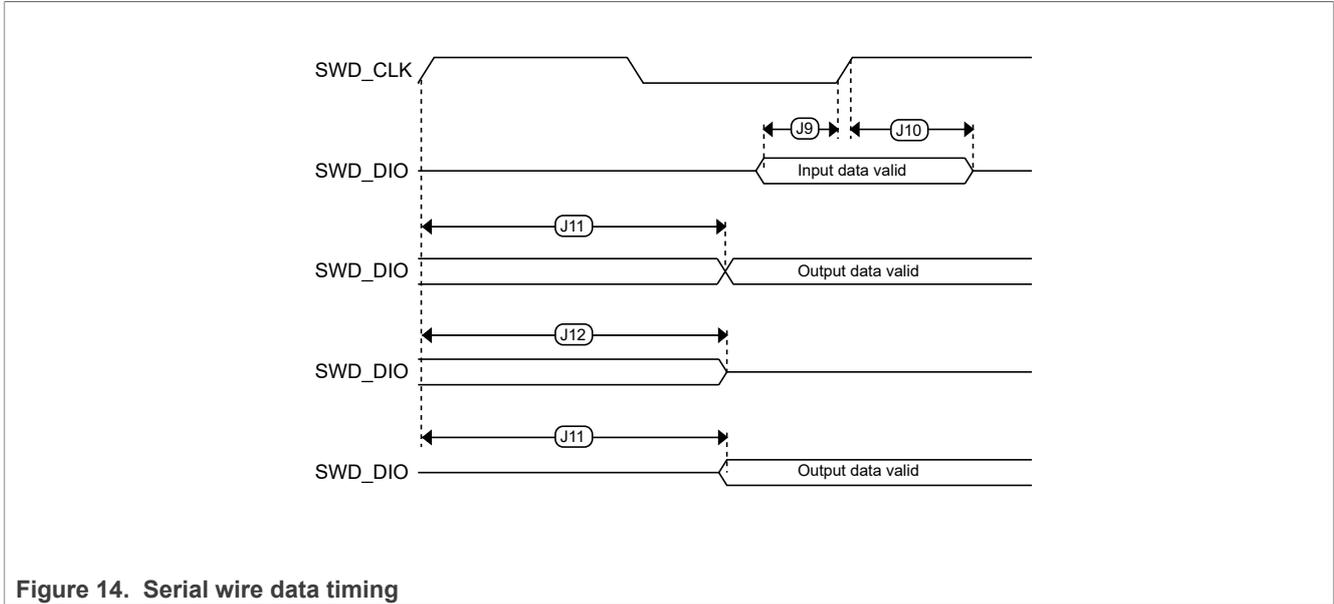


Figure 13. Serial wire clock input timing



6.2 External oscillator (OSC) and ICS characteristics

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	Characteristic	Symbol	Min	Typical ^[1]	Max	Unit	
1	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
		High range (RANGE = 1)	f_{hi}	4	—	24	MHz
2	Load capacitors	C1, C2	See Note ^[2]				
3	Feedback resistor	Low Frequency, Low-Power Mode ^[3]	R_F	—	—	—	MΩ
		Low Frequency, High-Gain Mode		—	10	—	MΩ
		High Frequency, Low-Power Mode		—	1	—	MΩ
		High Frequency, High-Gain Mode		—	1	—	MΩ
4	Series resistor - Low Frequency	Low-Power Mode ^[3]	R_S	—	0	—	kΩ
		High-Gain Mode		—	200	—	kΩ
5	Series resistor - High Frequency	Low-Power Mode ^[3]	R_S	—	0	—	kΩ
		Series resistor - High Frequency, High-Gain Mode		—	0	—	kΩ
	4 MHz	—		0	—	kΩ	
	8 MHz	—		0	—	kΩ	
6	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal ^{[4],[5]}	Low range, low power	t_{CSTL}	—	1000	—	ms
		Low range, high gain		—	800	—	ms
		High range, low power	t_{CSTH}	—	3	—	ms
		High range, high gain		—	1.5	—	ms

Table 9. OSC and ICS specifications (temperature range = -40 to 1

Num	Characteristic	Symbol	Min	Typical ^[1]	Max	Unit	
7	Internal reference start-up time	t_{IRST}	—	20	50	μs	
8	Internal reference clock (IRC) frequency trim range	f_{int_t}	31.25	—	39.0625	kHz	
9	Internal reference clock frequency, factory trimmed'	f_{int_ft}	—	37.5	—	kHz	
10	DCO output frequency range	FLL reference = f_{int_t} , flo, or $f_{hi}/RDIV$	f_{dco}	40	—	50	MHz
11	Factory trimmed internal oscillator accuracy	Δf_{int_ft}	-0.8	—	0.8	%	
12	Deviation of IRC over temperature when trimmed at $T = 25\text{ }^{\circ}C$, $V_{DD} = 5\text{ V}$	Over temperature range from $-40\text{ }^{\circ}C$ to $125\text{ }^{\circ}C$	Δf_{int_t}	-1	—	0.8	%
13	Frequency accuracy of DCO output using factory trim value	Over temperature range from $-40\text{ }^{\circ}C$ to $125\text{ }^{\circ}C$	Δf_{dco_ft}	-2.3	—	0.8	%
14	FLL acquisition time ^{[4],[6]}	$t_{Acquire}$	—	—	2	ms	
15	Long term jitter of DCO output clock (averaged over 2 ms interval) ^[7]	C_{Jitter}	—	0.02	0.2	% f_{dco}	

- [1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
- [2] See crystal or resonator manufacturer's recommendation.
- [3] Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
- [4] This parameter is characterized and not tested on each device.
- [5] Proper PC board layout procedures must be followed to achieve specifications.
- [6] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- [7] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

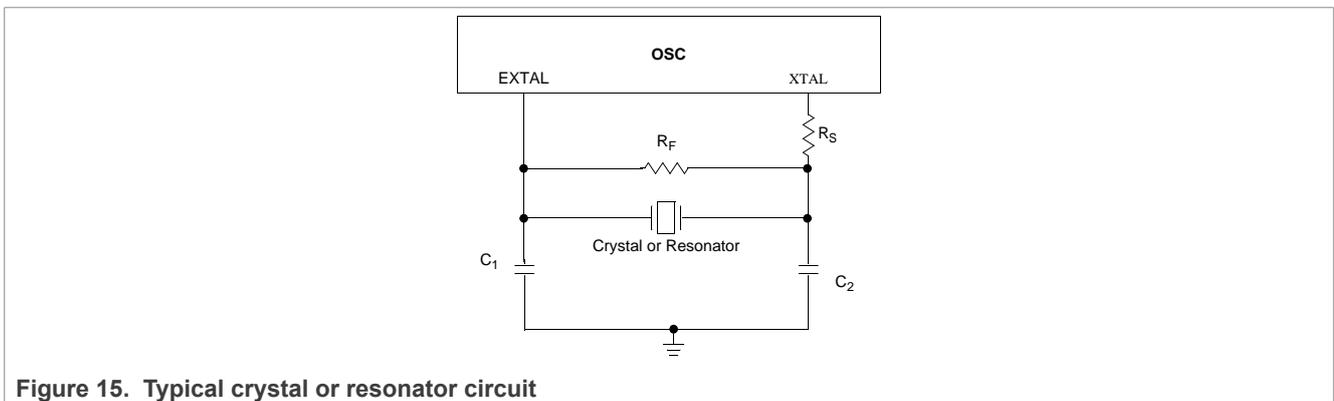


Figure 15. Typical crystal or resonator circuit

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 10. Flash characteristics

Characteristic	Symbol	Min ^[1]	Typical ^[2]	Max ^[3]	Unit ^[4]
Supply voltage for program/erase -40 °C to 125 °C	V _{prog/erase}	2.7	—	5.5	V
Supply voltage for read operation	V _{Read}	2.7	—	5.5	V
NVM Bus frequency	f _{NVMBUS}	1	—	24	MHz
NVM Operating frequency	f _{NVMOP}	0.8	1	1.05	MHz
Erase Verify All Blocks	t _{VFYALL}	—	—	2605	t _{cyc}
Erase Verify Flash Block	t _{RD1BLK}	—	—	2579	t _{cyc}
Erase Verify Flash Section	t _{RD1SEC}	—	—	485	t _{cyc}
Read Once	t _{RDONCE}	—	—	464	t _{cyc}
Program Flash (2 word)	t _{PGM2}	0.12	0.13	0.31	ms
Program Flash (4 word)	t _{PGM4}	0.21	0.21	0.49	ms
Program Once	t _{PGMONCE}	0.20	0.21	0.21	ms
Erase All Blocks	t _{ERSALL}	95.42	100.18	100.30	ms
Erase Flash Block	t _{ERSBLK}	95.42	100.18	100.30	ms
Erase Flash Sector	t _{ERSPG}	19.10	20.05	20.09	ms
Unsecure Flash	t _{UNSECU}	95.42	100.19	100.31	ms
Verify Backdoor Access Key	t _{VFYKEY}	—	—	482	t _{cyc}
Set User Margin Level	t _{MLOADU}	—	—	415	t _{cyc}
FLASH Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	10 k	100 k	—	Cycles
Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles	t _{D_ret}	15	100	—	years

[1] Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
 [2] Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
 [3] Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
 [4] t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

Table 12. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	Symbol	Min	Typ ^[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDA}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	582	990	μA
Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)		1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	40	—	
Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	23.5	—	
Total unadjusted Error ^[2]	12-bit mode	E_{TUE}	—	± 5.0	—	LSB ^[3]
	10-bit mode		—	± 1.5	—	
	8-bit mode		—	± 0.8	—	
Differential Non-Linearity	12-bit mode	DNL	—	± 1.5	—	LSB ^[3]
	10-bit mode		—	± 0.4	—	
	8-bit mode		—	± 0.15	—	
Integral Non-Linearity	12-bit mode	INL	—	± 1.5	—	LSB ^[3]
	10-bit mode		—	± 0.4	—	
	8-bit mode		—	± 0.15	—	
Zero-scale error ^[4]	12-bit mode	E_{ZS}	—	± 1.0	—	LSB ^[3]
	10-bit mode		—	± 0.2	—	
	8-bit mode		—	± 0.35	—	

Table 12. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$).

Characteristic	Conditions	Symbol	Min	Typ ^[1]	Max	Unit
Full-scale error ^[5]	12-bit mode	E_{FS}	—	±2.5	—	LSB ^[3]
	10-bit mode		—	±0.3	—	
	8-bit mode		—	±0.25	—	
Quantization error	≤12 bit modes	E_Q	—	—	±0.5	LSB ^[3]
Input leakage error ^[6]	all modes	E_{IL}	$I_{in} \times R_{AS}$			mV
Temp sensor slope	-40 °C–25 °C	m	—	3.266	—	mV/°C
	25 °C–125 °C		—	3.638	—	
Temp sensor voltage	25 °C	V_{TEMP25}	—	1.396	—	V

- [1] Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- [2] Includes quantization
- [3] $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
- [4] $V_{ADIN} = V_{SSA}$
- [5] $V_{ADIN} = V_{DDA}$
- [6] I_{in} = leakage current (refer to DC characteristics)

6.4.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DDA}	2.7	—	5.5	V
Supply current (Operation mode)	I_{DDA}	—	10	20	µA
Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
Analog input offset voltage	V_{AIO}	—	—	40	mV
Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
Propagation Delay	t_D	—	0.4	1	µs

6.5 Communication interfaces

6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD} , unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

Table 14. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{BUS}/2048$	$f_{BUS}/2$	Hz	f_{BUS} is the bus clock

Table 14. SPI master mode timing...continued

Num.	Symbol	Description	Min.	Max.	Unit	Comment
2	t_{SPSCK}	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	t_{SU}	Data setup time (inputs)	8	—	ns	—
7	t_{HI}	Data hold time (inputs)	8	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	20	—	ns	—
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

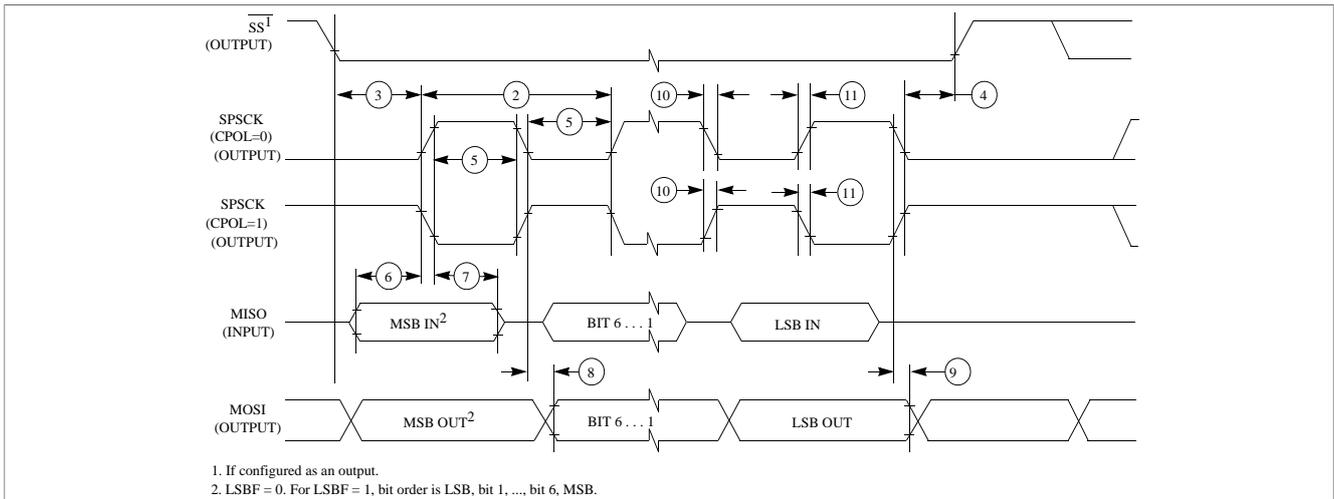


Figure 17. SPI master mode timing (CPHA=0)

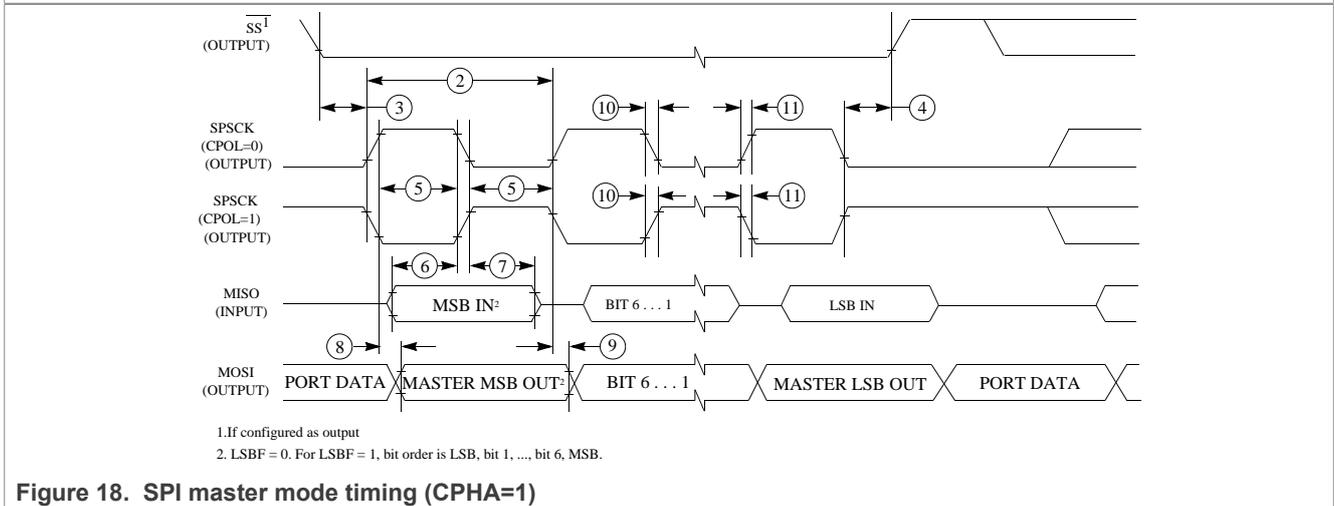
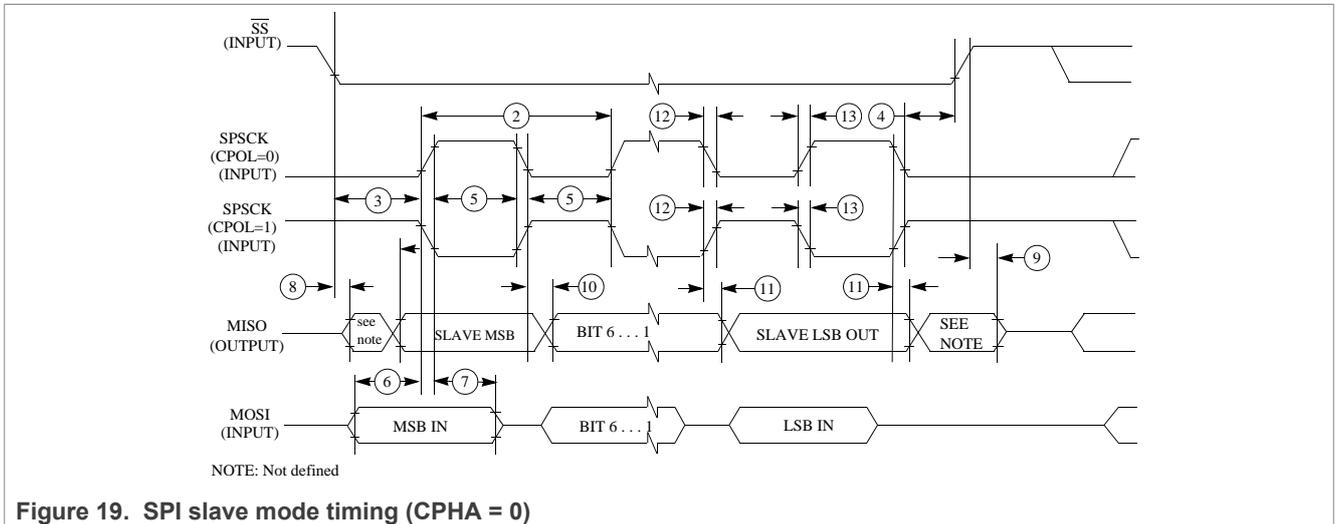


Figure 18. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{BUS}/4$	Hz	f_{BUS} is the bus clock as defined in Table 5 .
2	t_{SPSCK}	SPSCK period	$4 \times t_{BUS}$	—	ns	$t_{BUS} = 1/f_{BUS}$
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{BUS} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{BUS} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



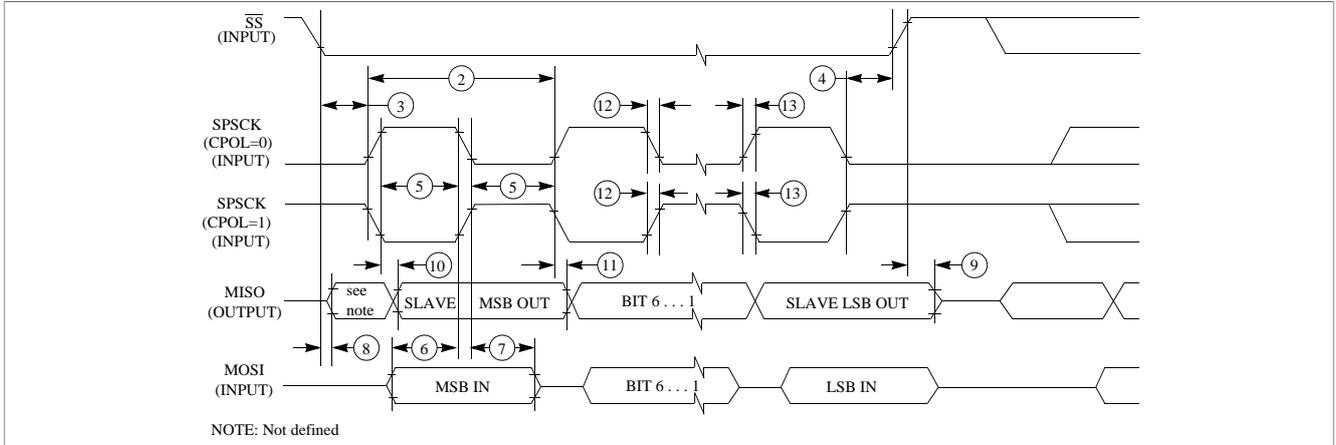


Figure 20. SPI slave mode timing (CPHA=1)

6.5.2 MSCAN

Table 16. MSCAN wake-up pulse characteristics

Parameter	Symbol	Min	Typ	Max	Unit
MSCAN wakeup dominant pulse filtered	t_{WUP}	-	-	1.5	μs
MSCAN wakeup dominant pulse pass	t_{WUP}	5	-	-	μs

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing’s document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23237W

8 Pinout

8.1 Signal multiplexing and pin assignments

For the pin muxing details see section Signal Multiplexing and Signal Descriptions of KEA128 Reference Manual.

9 Revision History

The following table provides a revision history for this document.

Table 17. Revision History

Document ID	Release date	Description
S9KEA64P64M20SF0 v. 6	30 January 2024	<ul style="list-style-type: none"> In Section 3.3 modified the 'Description' and 'Values' in 'Field' M.
S9KEA64P64M20SF0 v. 5	23 September 2019	<ul style="list-style-type: none"> Added row T_{ramp} in Table 2.
S9KEA64P64M20SF0 v. 4	03 Sept 2014	<ul style="list-style-type: none"> Data Sheet type changed to "Technical Data".
S9KEA64P64M20SF0 v. 3	18 July 2014	<ul style="list-style-type: none"> Added supported part numbers. Section 4.3 section is updated. Figures in Section 5.1.1 section are updated. Specs updated in following tables: <ul style="list-style-type: none"> – Table 9.
S9KEA64P64M20SF0 v. 2	18 June 2014	<ul style="list-style-type: none"> Parameter Classification section is removed. Classification column is removed from all the tables in the document. New section added - Section 5.1.2.
S9KEA64P64M20SF0 v. 1	11 March 2014	Initial Release

10 Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

10.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

10.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security- Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

10.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile — are trademarks and/or registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

KEA128 Sub-Family Data Sheet Supports the following: S9KEAZ64AMLK(R), S9KEAZ128AMLK(R), S9KEAZ64AVLK(R), S9KEAZ128AVLK(R), S9KEAZ64ACLK(R), S9KEAZ128ACLK(R), S9KEAZ64AMLH(R), S9KEAZ128AMLH(R), S9KEAZ64AVLH(R), S9KEAZ128AVLH(R), S9KEAZ64ACLH(R) and S9KEAZ128ACLH(R)

Contents

1 Key features 1

1.1 Operating characteristics 1

1.2 Performance 1

1.3 Memories and memory interfaces 1

1.4 Clocks 1

1.5 System peripherals 1

1.6 Security and integrity modules 2

1.7 Human-machine interface 2

1.8 Analog modules 2

1.9 Timers 2

1.10 Communication interfaces 2

1.11 Package options 2

2 Ordering parts 2

2.1 Determining valid orderable parts 2

3 Part identification 2

3.1 Description 2

3.2 Format 3

3.3 Fields 3

3.4 Example 3

4 Ratings 3

4.1 Thermal handling ratings 3

4.2 Moisture handling ratings 4

4.3 ESD handling ratings 4

4.4 Voltage and current operating ratings 4

5 General 5

5.1 Nonswitching electrical specifications 5

5.1.1 DC characteristics 5

5.1.2 Supply current characteristics 11

5.1.3 EMC performance 13

5.2 Switching specifications 13

5.2.1 Control timing 13

5.2.2 FTM module timing 14

5.3 Thermal specifications 15

5.3.1 Thermal characteristics 15

6 Peripheral operating requirements and behaviors 16

6.1 Core modules 16

6.1.1 SWD electricals 16

6.2 External oscillator (OSC) and ICS characteristics 17

6.3 NVM specifications 19

6.4 Analog 20

6.4.1 ADC characteristics 20

6.4.2 Analog comparator (ACMP) electricals 22

6.5 Communication interfaces 22

6.5.1 SPI switching specifications 22

6.5.2 MSCAN 25

7 Dimensions 25

7.1 Obtaining package dimensions 25

8 Pinout 25

8.1 Signal multiplexing and pin assignments 25

9 Revision History 25

10 Legal information 27

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.