MAX3232E-Q1 Automotive 3V TO 5.5V Multichannel RS-232 Line Driver and Receiver WITH ±15kV IEC ESD Protection

1 Features

- Qualified for automotive applications
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates with 3V to 5.5V V_{CC} supply
- Operates up to 250kbit/s
- Two drivers and two receivers
- Low standby current: 300µA Typical
- External capacitors: 4 × 0.1µF
- Accepts 5V logic input with 3.3V supply
- Pin compatible to alternative high-speed pin-compatible device (1Mbit/s): SNx5C3232

2 Applications

- Industrial PCs
- Wired networking
- Data center and enterprise computing
- Battery-powered systems
- Notebooks
- Palmtop PCs
- Hand-held equipment

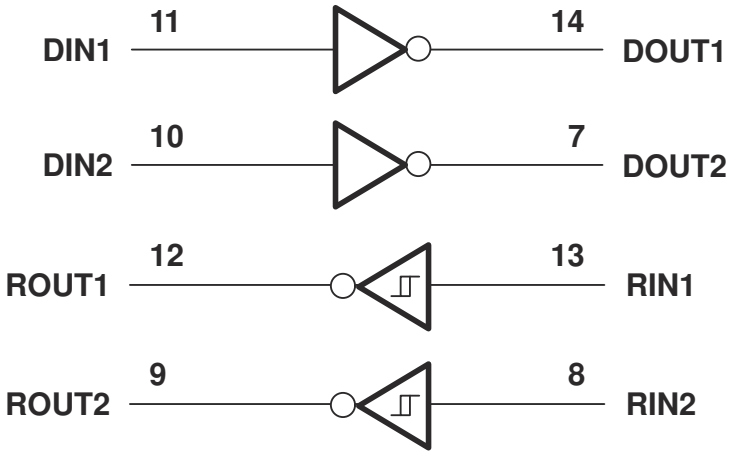
3 Description

The MAX3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The device operates at data signaling rates up to 250kbit/s and a maximum of 30V/µs driver output slew rate.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
MAX3232E	PW (TSSOP, 16)	5mm x 6.4mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

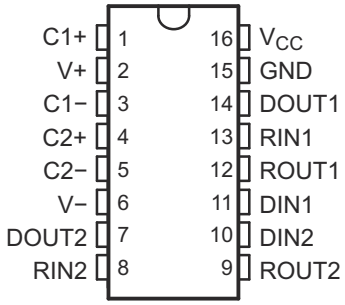


Figure 4-1. PW Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V+	2	O	Positive charge pump output for storage capacitor only
C1–	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2–	5	—	Negative lead of C2 capacitor
V–	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 3V to 5.5V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Drivers	–0.3	6	V
		Receivers	–25	25	V
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	V
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 Recommended Operating Conditions

see Figure 6-1 (1)

				MIN	NOM	MAX	UNIT
	Supply voltage	V_{CC} = 3.3V		3	3.3	3.6	V
		V_{CC} = 5V		4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3V	2		5.5	V
			V_{CC} = 5V	2.4		5.5	
V_{IL}	Driver low-level input voltage	DIN		0		0.8	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	MAX3232I		–40		85	°C

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ±0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ±0.5V.

5.3 Thermal Information

THERMAL METRIC(1)		TSSOP (PW)	UNIT
		16-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-1)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 3.3V or 5V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V and T_A = 25°C.

5.5 Driver Section, Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-1)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3kΩ to GND, DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3kΩ to GND, DIN = V_{CC}		–5.4	–5	V
I_{IH}	High-level input current	V_I = V_{CC}		±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND		±0.01	±1	µA
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6V, V_O = 0V		±35	±60	mA
		V_{CC} = 5.5V, V_O = 0V				
r_o	Output resistance	V_{CC}, V+, and V– = 0V, V_O = 2V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

5.6 Driver Section, Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-1)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 1000pF, One DOUT switching, R_L = 3kΩ, See Figure 6-1		150	250		kbit/s
$t_{sk(p)}$	Pulse skew(3)	C_L = 150pF to 2500pF, R_L = 3kΩ to 7kΩ, See Figure 6-2			300		ns
SR(tr)	Slew rate, transition region (see Figure 6-1)	R_L = 3kΩ to 7kΩ, V_{CC} = 3.3V	C_L = 150pF to 1000pF	6		30	v/µs
			C_L = 150pF to 2500pF	4		30	

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

5.7 Receiver Section, Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-1)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA	V_{CC} – 0.6V	V_{CC} – 0.1V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3V		1.5	2.4	V
		V_{CC} = 5V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3V	0.6	1.2		V
		V_{CC} = 5V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_I	Input resistance	V_I = ±3V to ±25	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V and T_A = 25°C.

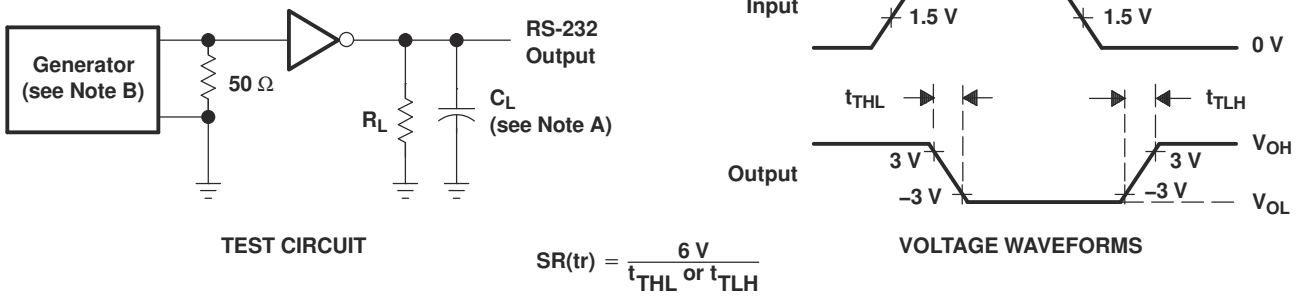
5.8 Receiver Section, Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-3)

PARAMETER		TEST CONDITIONS(1)	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150pF	300	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150pF	300	ns
$t_{sk(p)}$	Pulse skew(3)		300	ns

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

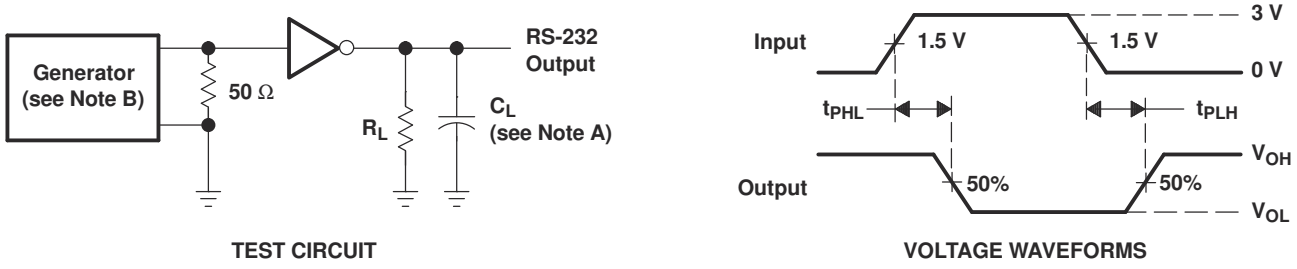
Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250kbit/s, Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

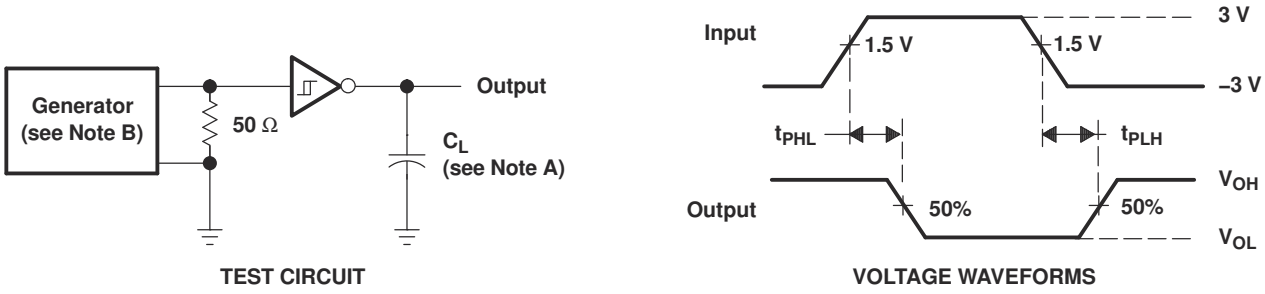
Figure 6-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250kbit/s, Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

Figure 6-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

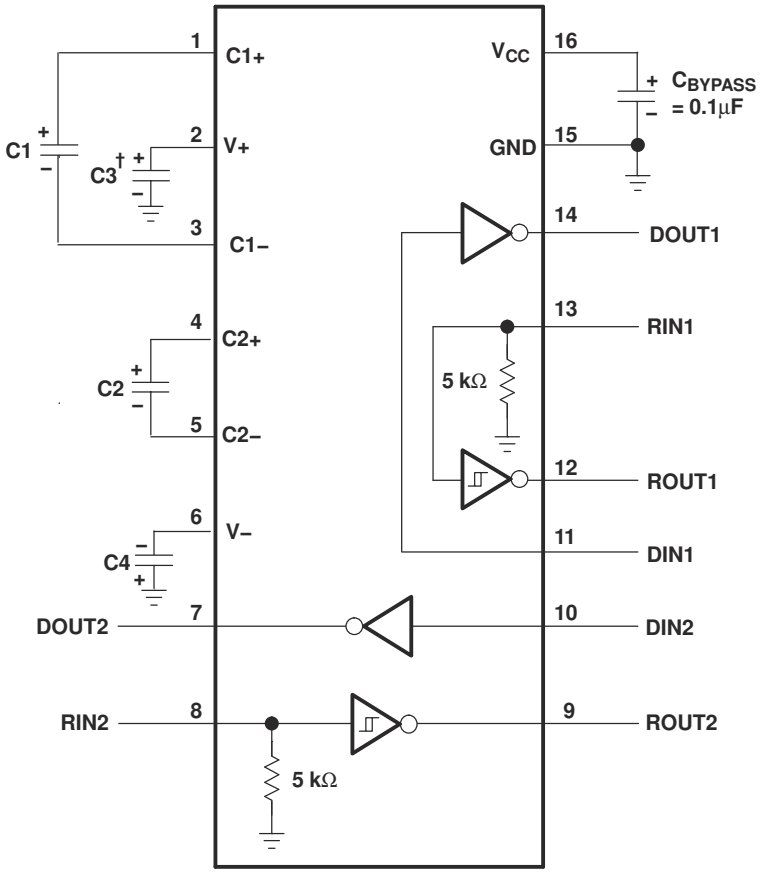
Figure 6-3. Receiver Propagation Delay Times

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.
B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6-1. Typical Operating Circuit and Capacitor Values

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

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7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2008) to Revision B (December 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Thermal Information* table	4
• Changed V_{OL}: moved –5V from the MIN to the MAX column in *Driver Section, Electrical Characteristics*	5

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3232EIPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3232I
MAX3232EIPWRQ1.Z	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3232I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF MAX3232E-Q1 :

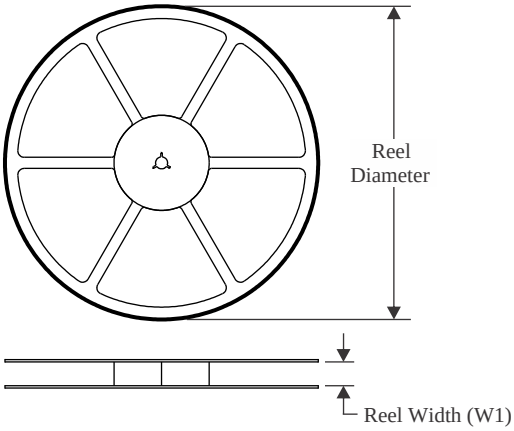
- Catalog : MAX3232E

NOTE: Qualified Version Definitions:

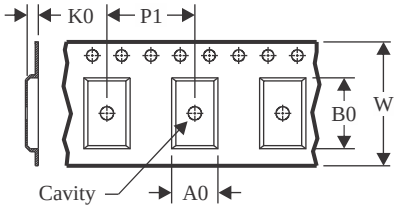
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

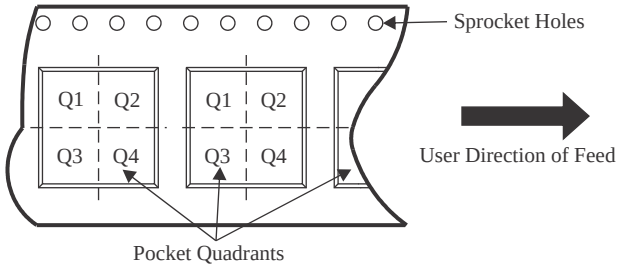


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

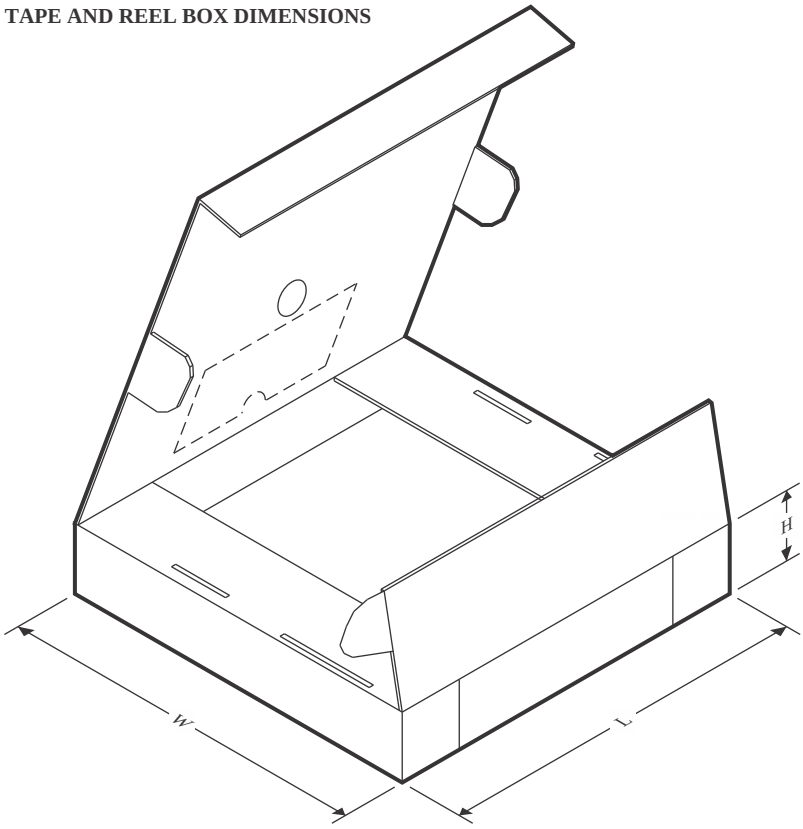
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3232EIPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

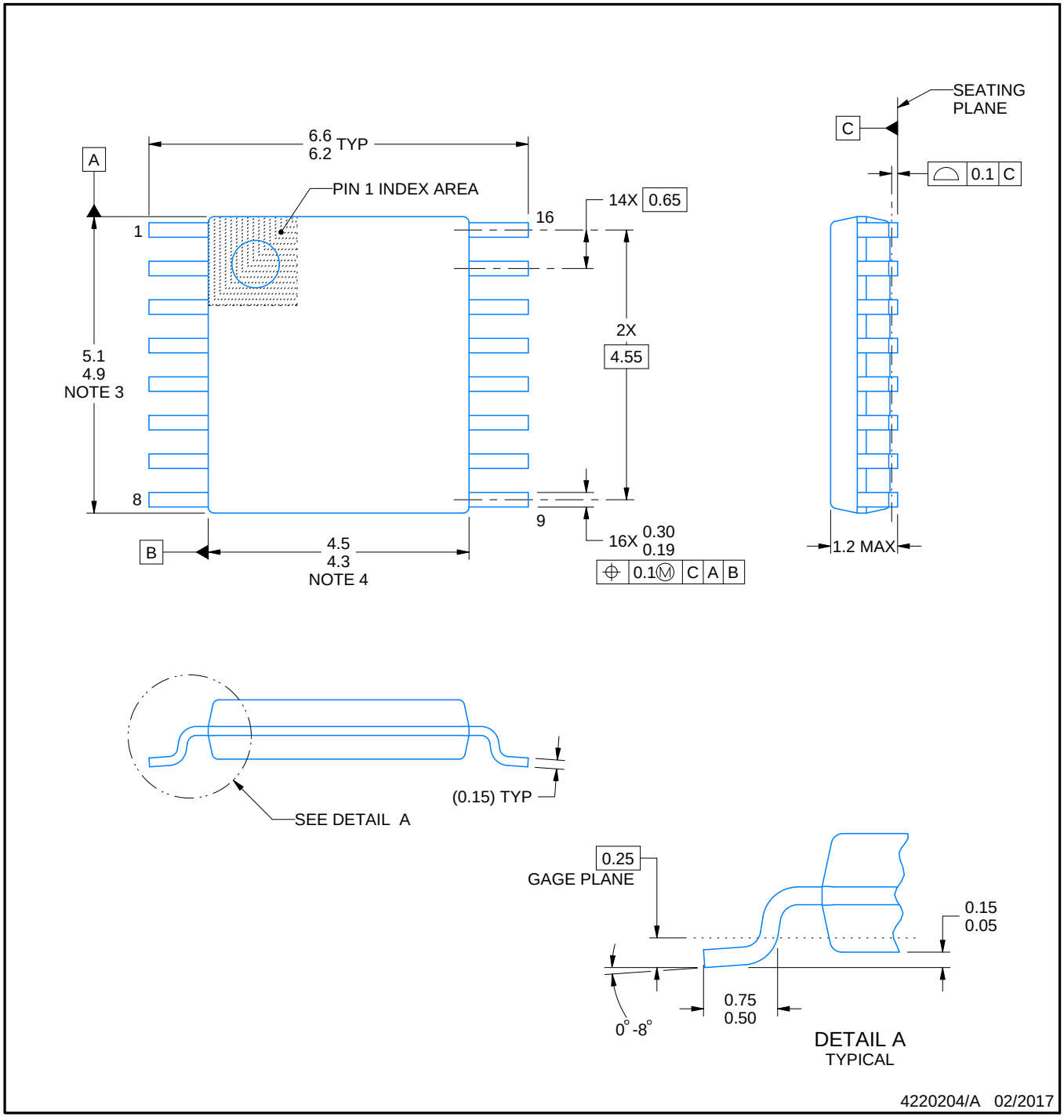
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3232EIPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0016A

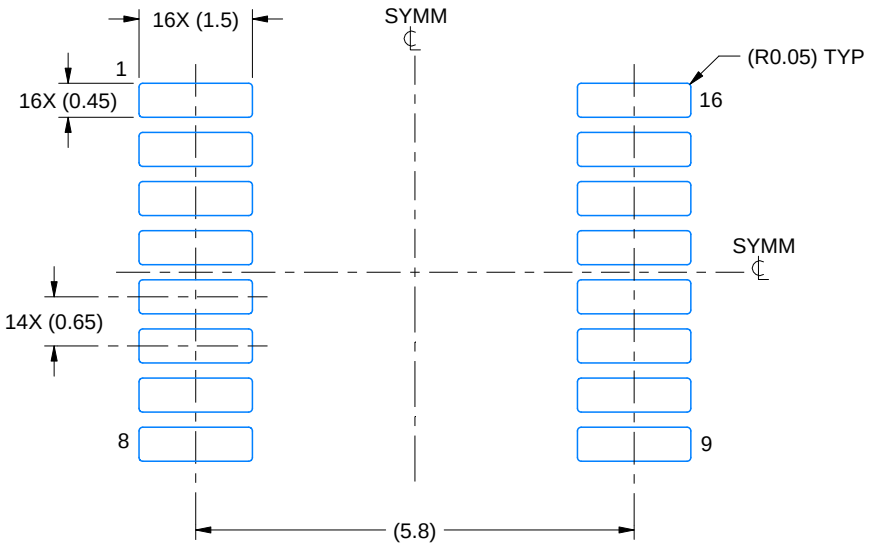
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

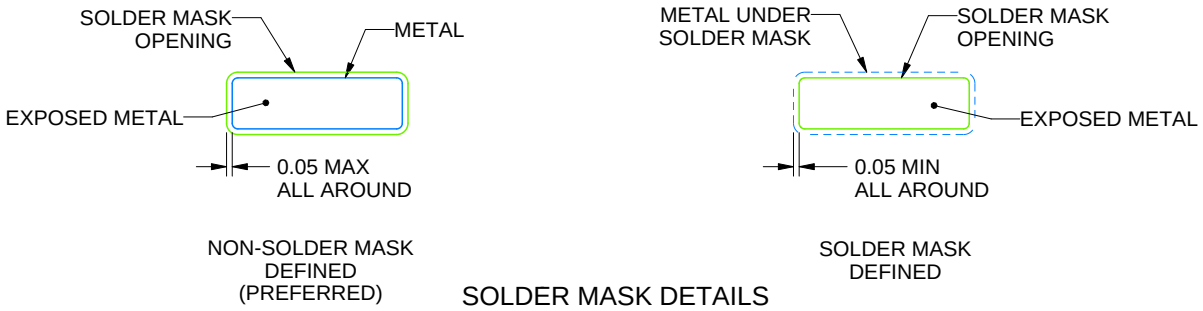


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

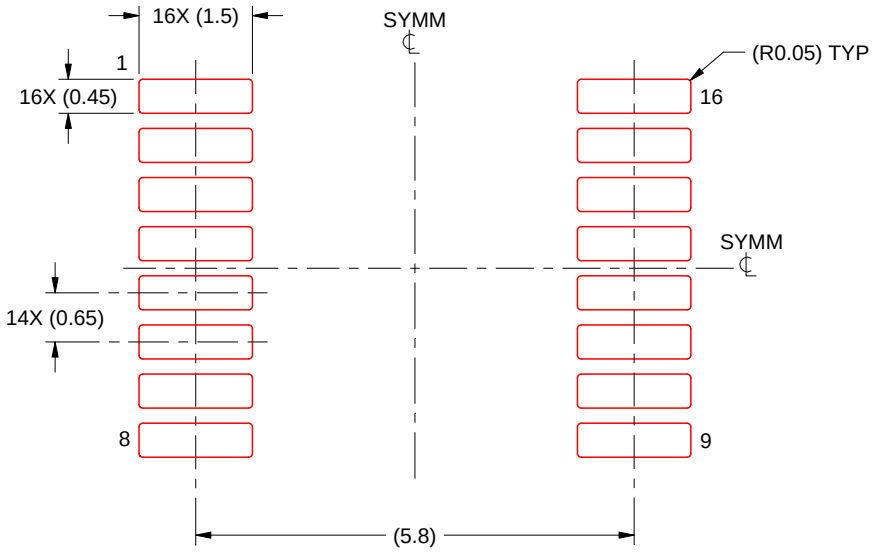


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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