

74LVC1G3157

10 Ω single-pole double-throw analog switch

Rev. 11 — 23 August 2023

Product data sheet

1. General description

The 74LVC1G3157 is a single-pole double-throw analog switch with a digital select input (S), two independent inputs/outputs (Y0 and Y1) and a common input/output (Z). Control inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at control inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V
- 32 mA continuous switch current
- Break-before-make switching
- High noise immunity
- CMOS low power dissipation
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD 78 Class I
- Overvoltage tolerant control inputs to 5.5 V
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G3157GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74LVC1G3157GV	-40 °C to +125 °C	SC-74; TSOP6	plastic surface-mounted package; 6 leads	SOT457
74LVC1G3157GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G3157GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G3157GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G3157GX	-40 °C to +125 °C	X2SON6	plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 × 0.8 × 0.32 mm	SOT1255-2

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G3157GW	YJ
74LVC1G3157GV	YJ
74LVC1G3157GM	YJ
74LVC1G3157GN	YJ
74LVC1G3157GS	YJ
74LVC1G3157GX	YJ

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

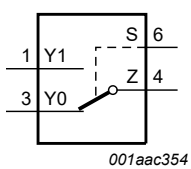


Fig. 1. Logic symbol

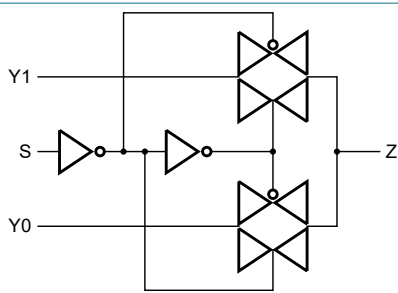
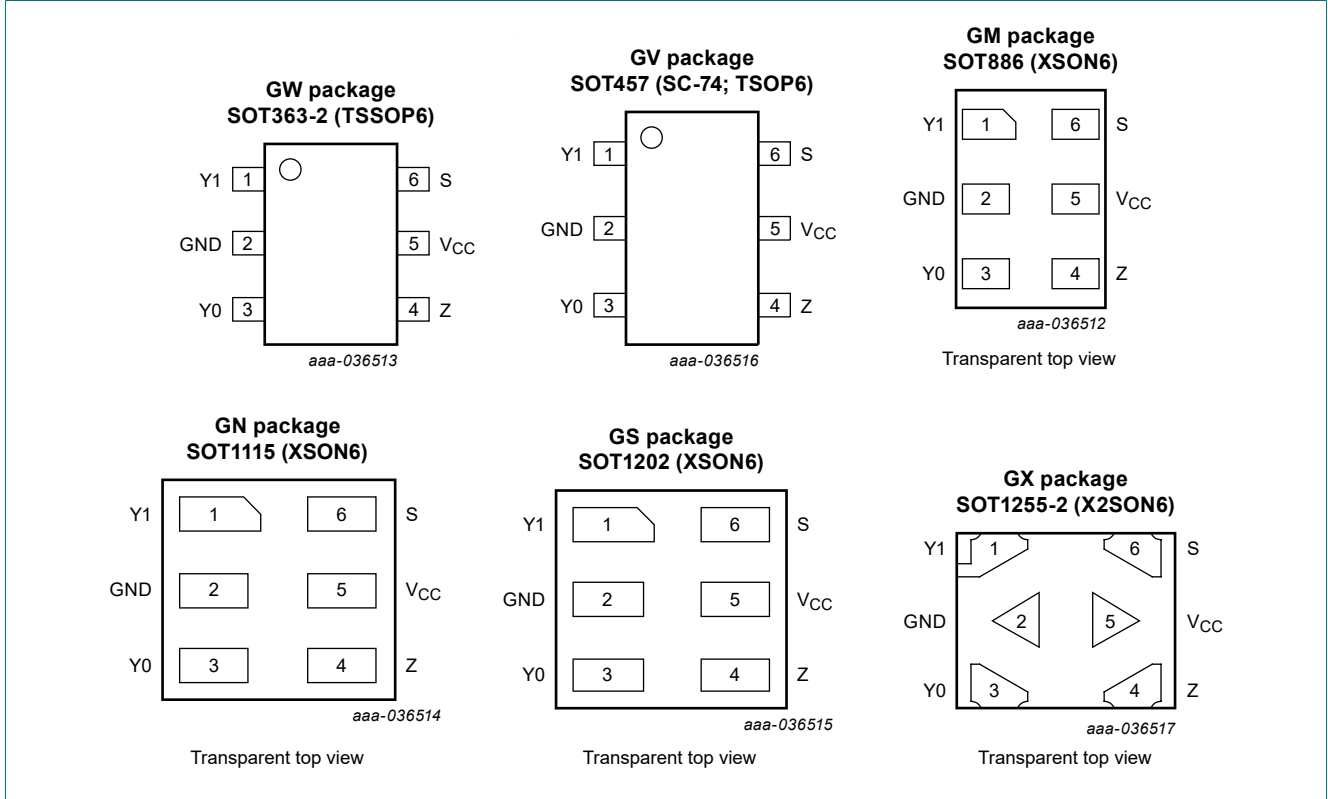


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y1	1	independent input or output
GND	2	ground (0 V)
Y0	3	independent input or output
Z	4	common output or input
V _{CC}	5	supply voltage
S	6	select input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input S	Channel on
L	Y0
H	Y1

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	$V_{CC} + 0.5$	V
I_{SW}	switch current	$V_{SW} > -0.5\text{ V}$ or $V_{SW} < V_{CC} + 0.5\text{ V}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$
P_{tot}	total power dissipation	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 $^{\circ}\text{C}$.

For SOT457 (SC-74; TSOP6) package: P_{tot} derates linearly with 4.1 mW/K above 89 $^{\circ}\text{C}$.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 $^{\circ}\text{C}$.

For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 $^{\circ}\text{C}$.

For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 $^{\circ}\text{C}$.

For SOT1255-2 (X2SON6) package: P_{tot} derates linearly with 3.3 mW/K above 75 $^{\circ}\text{C}$.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	enable and disable mode [1]	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V}$ to 2.7 V [2]	-	-	20	ns/V
		$V_{CC} = 2.7\text{ V}$ to 5.5 V [2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	0.7 × V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	-	0.3 × V _{CC}	V
I _I	input leakage current	pin S; V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V [2]	-	±0.1	±1	-	±1	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; see Fig. 3 [2]	-	±0.1	±0.2	-	±0.5	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; see Fig. 4 [2]	-	±0.1	±1	-	±2	μA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{SW} = GND or V _{CC} ; V _{CC} = 1.65 V to 5.5 V [2]	-	0.1	4	-	4	μA
ΔI _{CC}	additional supply current	pin S; V _I = V _{CC} - 0.6 V; V _{CC} = 5.5 V; V _{SW} = GND or V _{CC} [2]	-	5	500	-	500	μA
C _I	input capacitance		-	2.5	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	6.0	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	18	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C.
- [2] These typical values are measured at V_{CC} = 3.3 V.

10.1. Test circuits

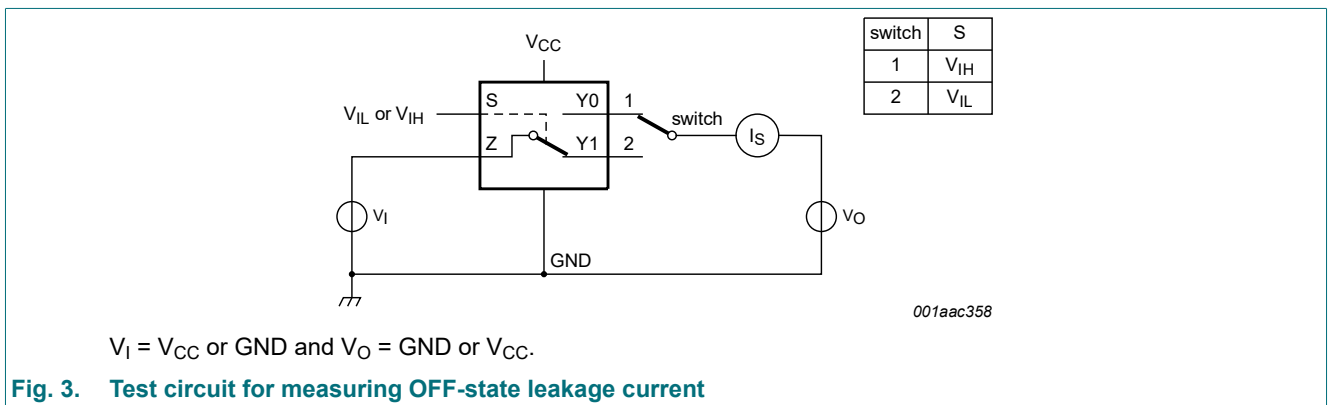
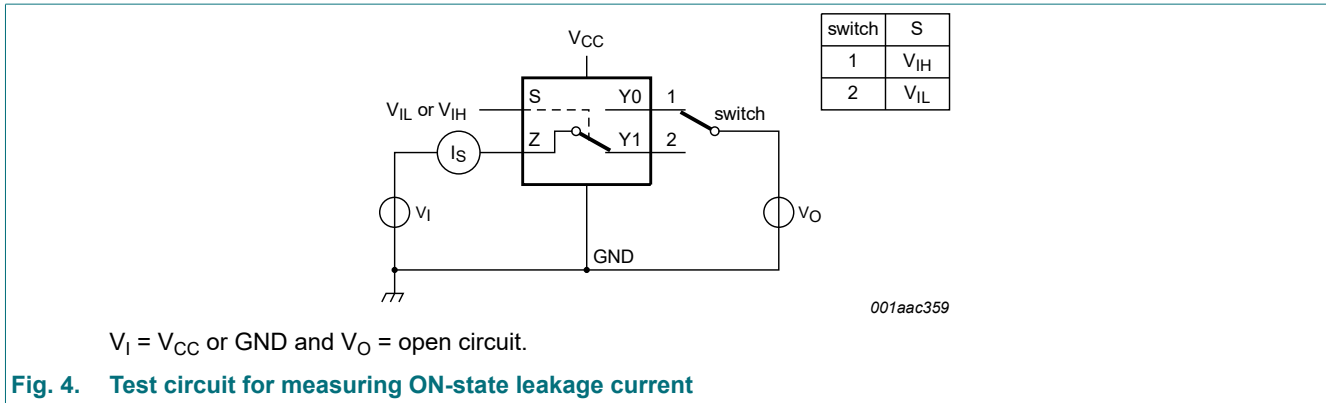


Fig. 3. Test circuit for measuring OFF-state leakage current



10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Fig. 6 to Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	$V_I = GND$ to V_{CC} ; see Fig. 5						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	34.0	130	-	195	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	12.0	30	-	45	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	10.4	25	-	38	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3$ V to 3.6 V	-	7.8	20	-	30	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	$V_I = GND$; see Fig. 5						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	8.2	18	-	27	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	7.1	16	-	24	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	6.9	14	-	21	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3$ V to 3.6 V	-	6.5	12	-	18	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	5.8	10	-	15	Ω
		$V_I = V_{CC}$; see Fig. 5						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	10.4	30	-	45	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	7.6	20	-	30	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	7.0	18	-	27	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3$ V to 3.6 V	-	6.1	15	-	23	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	4.9	10	-	15	Ω
R _{ON(flat)}	ON resistance (flatness)	$V_I = GND$ to V_{CC} [2]						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	26.0	-	-	-	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	5.0	-	-	-	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	3.5	-	-	-	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3$ V to 3.6 V	-	2.0	-	-	-	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	1.5	-	-	-	Ω

[1] Typical values are measured at $T_{amb} = 25$ °C and nominal V_{CC} .

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs

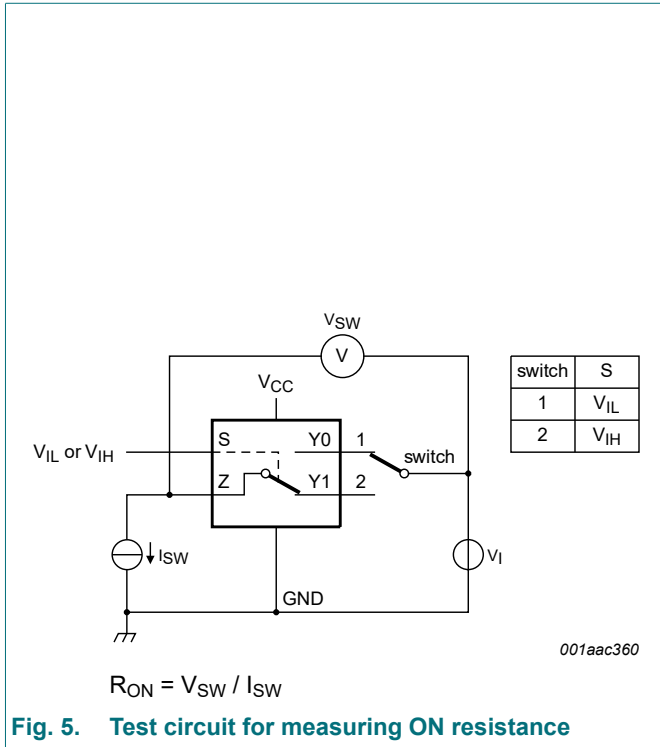


Fig. 5. Test circuit for measuring ON resistance

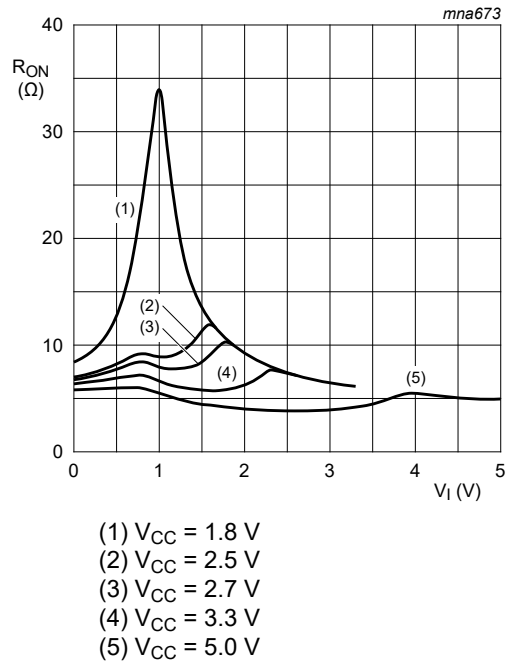


Fig. 6. Typical ON resistance as a function of input voltage; $T_{amb} = 25\text{ °C}$

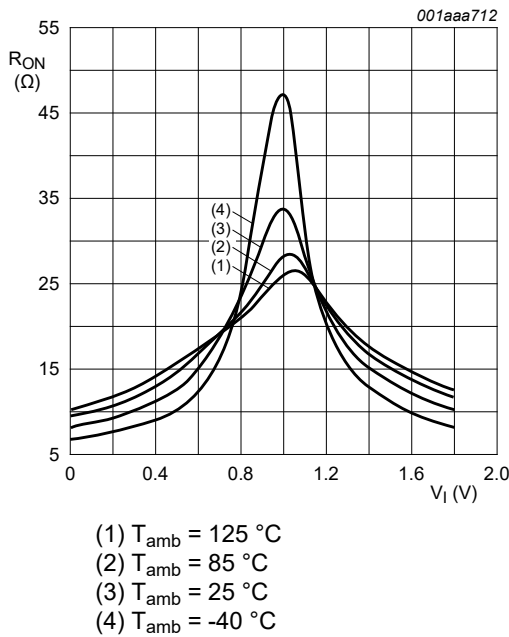


Fig. 7. ON resistance as a function of input voltage; $V_{CC} = 1.8\text{ V}$

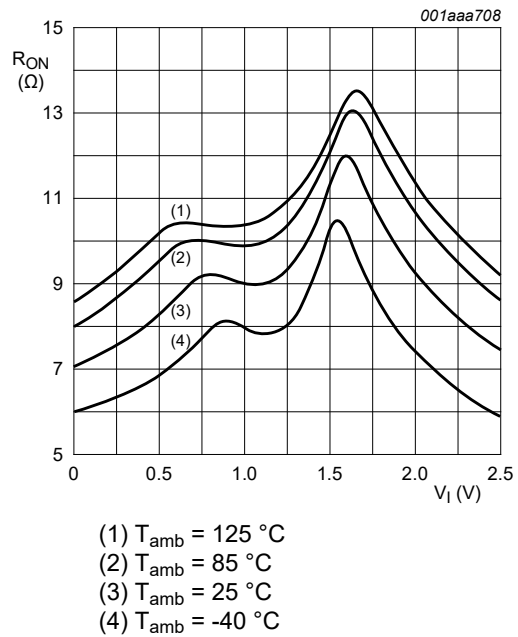


Fig. 8. ON resistance as a function of input voltage; $V_{CC} = 2.5\text{ V}$

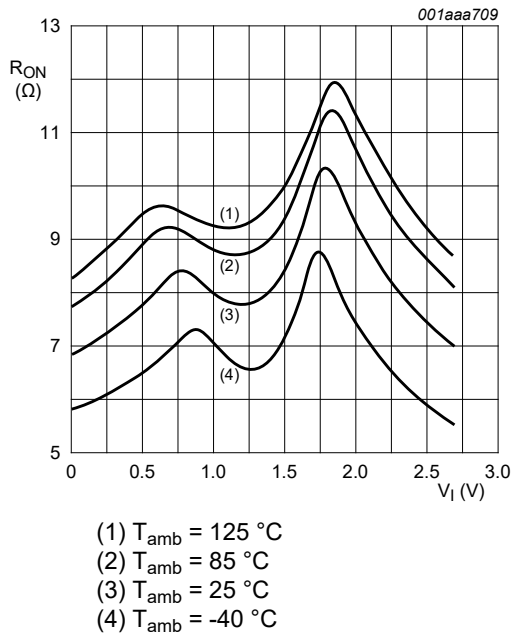


Fig. 9. ON resistance as a function of input voltage; $V_{CC} = 2.7\text{ V}$

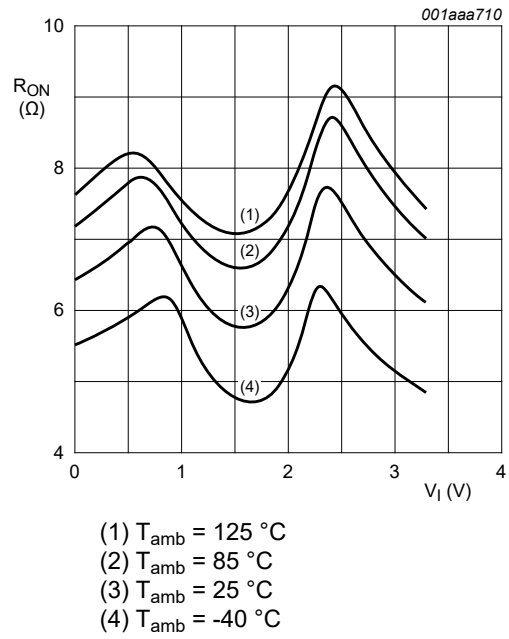


Fig. 10. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$

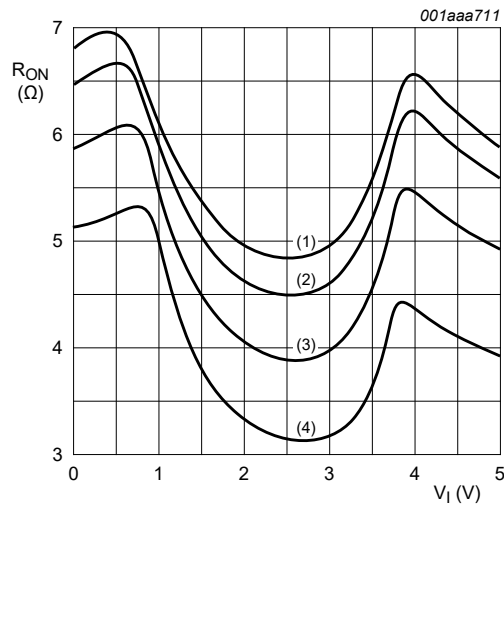


Fig. 11. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 15.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	Z to Yn or Yn to Z; see Fig. 12 [2] [3]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	2	-	3.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	1.2	-	2.0	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	1.0	-	1.5	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	1.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.6	-	1.0	ns
t_{en}	enable time	S to Yn; see Fig. 13 [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.1	8.7	20.8	3.1	22.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.2	5.3	11.5	2.2	12.5	ns
		$V_{CC} = 2.7 \text{ V}$	2.1	4.9	9.3	2.1	10.2	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	1.8	4.0	7.6	1.8	9.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.5	3.0	5.7	1.5	6.1	ns
t_{dis}	disable time	S to Yn; see Fig. 13 [5]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.0	6.0	11.4	3.0	11.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.1	4.4	7.3	2.1	7.6	ns
		$V_{CC} = 2.7 \text{ V}$	2.1	4.2	6.3	2.1	6.6	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	1.7	3.6	5.3	1.7	5.9	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.3	2.9	3.8	1.3	4.3	ns
t_{b-m}	break-before-make time	see Fig. 14 [6]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	-	-	0.5	-	ns

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and nominal V_{CC} .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

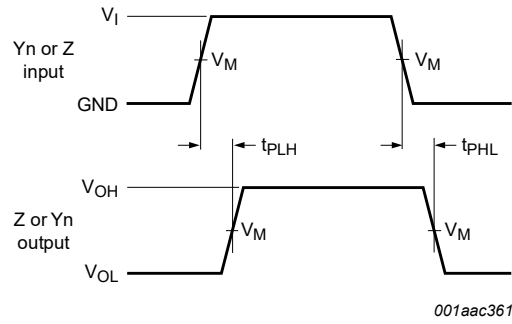
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

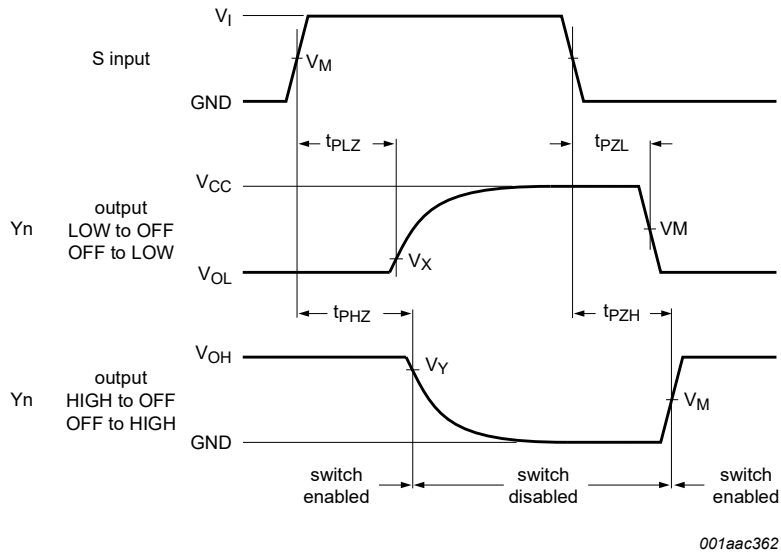
[6] Break-before-make specified by design.

11.1. Waveforms and test circuits



Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. Input (Yn or Z) to output (Z or Yn) propagation delays



Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

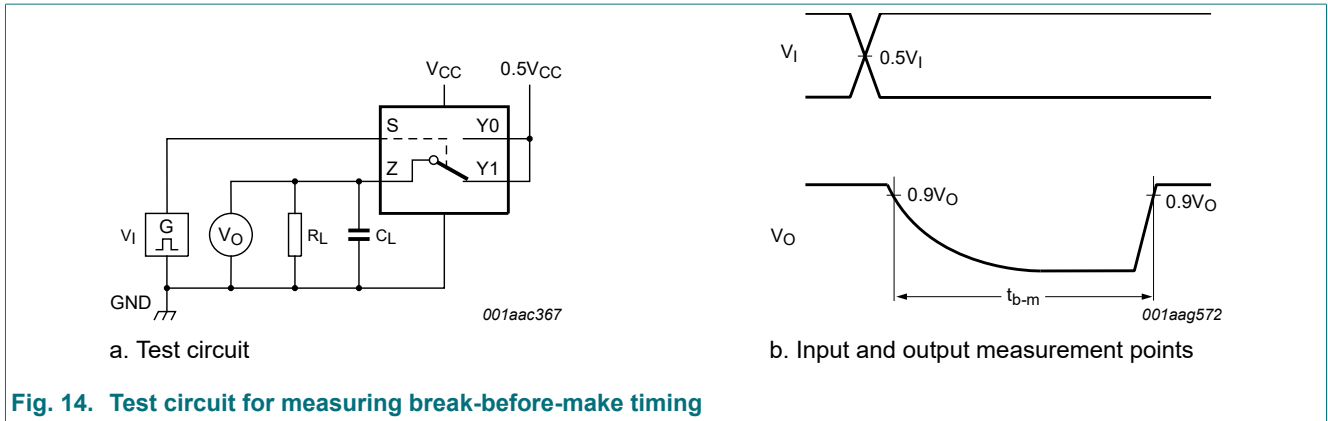


Fig. 14. Test circuit for measuring break-before-make timing

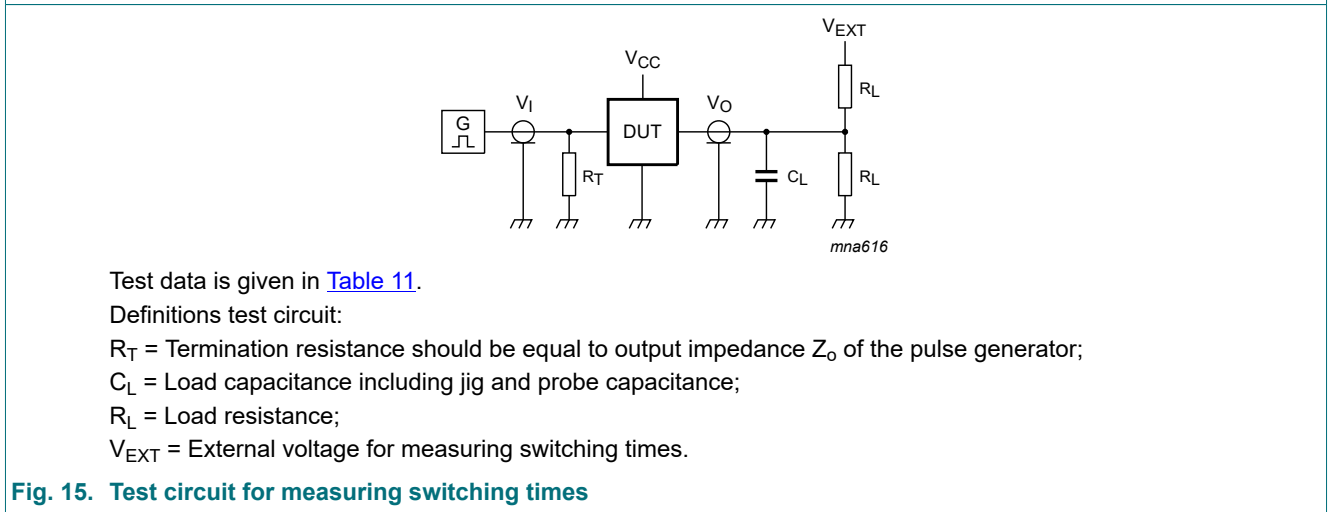


Fig. 15. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3 V to 3.6 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 600\text{ Hz to }20\text{ kHz}; R_L = 600\text{ }\Omega; C_L = 50\text{ pF}; V_i = 0.5\text{ V (p-p)}$; see Fig. 16				
		$V_{CC} = 1.65\text{ V}$	-	0.260	-	%
		$V_{CC} = 2.3\text{ V}$	-	0.078	-	%
		$V_{CC} = 3.0\text{ V}$	-	0.078	-	%
		$V_{CC} = 4.5\text{ V}$	-	0.078	-	%
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50\text{ }\Omega$; see Fig. 17				
		$V_{CC} = 1.65\text{ V}$	-	200	-	MHz
		$V_{CC} = 2.3\text{ V}$	-	300	-	MHz
		$V_{CC} = 3.0\text{ V}$	-	300	-	MHz
		$V_{CC} = 4.5\text{ V}$	-	300	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 50\text{ }\Omega; C_L = 5\text{ pF}; f_i = 10\text{ MHz}$; see Fig. 18				
		$V_{CC} = 1.65\text{ V}$	-	-42	-	dB
		$V_{CC} = 2.3\text{ V}$	-	-42	-	dB
		$V_{CC} = 3.0\text{ V}$	-	-40	-	dB
		$V_{CC} = 4.5\text{ V}$	-	-40	-	dB
Q_{inj}	charge injection	$C_L = 0.1\text{ nF}; V_{gen} = 0\text{ V}; R_{gen} = 0\text{ }\Omega; f_i = 1\text{ MHz}; R_L = 1\text{ M}\Omega$; see Fig. 19				
		$V_{CC} = 1.8\text{ V}$	-	3.3	-	pC
		$V_{CC} = 2.5\text{ V}$	-	4.1	-	pC
		$V_{CC} = 3.3\text{ V}$	-	5.0	-	pC
		$V_{CC} = 4.5\text{ V}$	-	6.4	-	pC
		$V_{CC} = 5.5\text{ V}$	-	7.5	-	pC

11.3. Test circuits

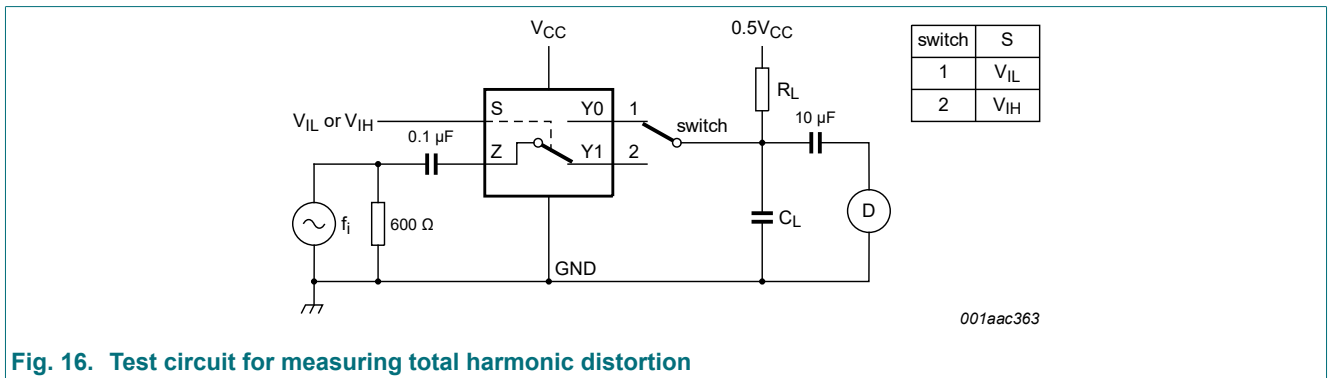
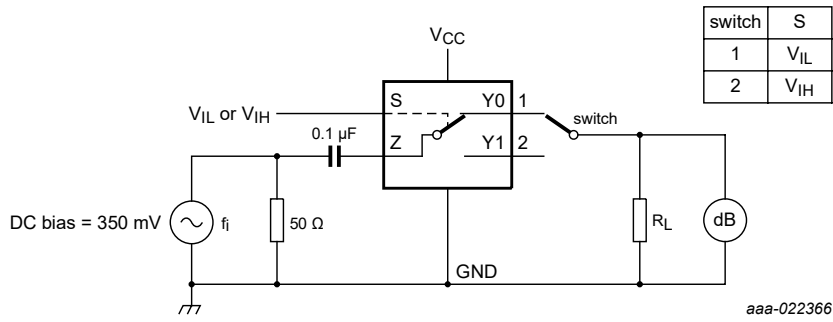
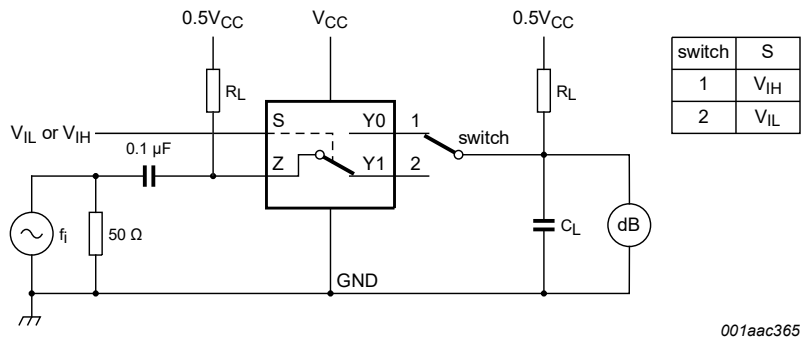


Fig. 16. Test circuit for measuring total harmonic distortion



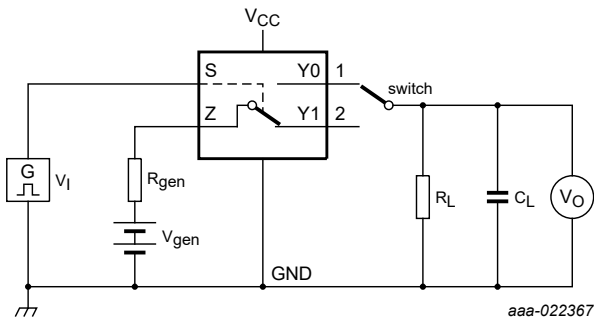
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 17. Test circuit for measuring the frequency response when switch is in ON-state



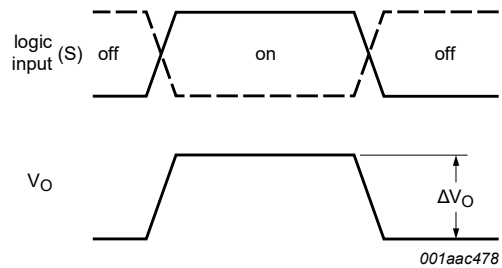
Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 18. Test circuit for measuring isolation (OFF-state)



a. Test circuit

- $Q_{inj} = \Delta V_O \times C_L$;
- ΔV_O = output voltage variation;
- R_{gen} = generator resistance;
- V_{gen} = generator voltage.



b. Input and output pulse definitions

Fig. 19. Test circuit for measuring charge injection

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

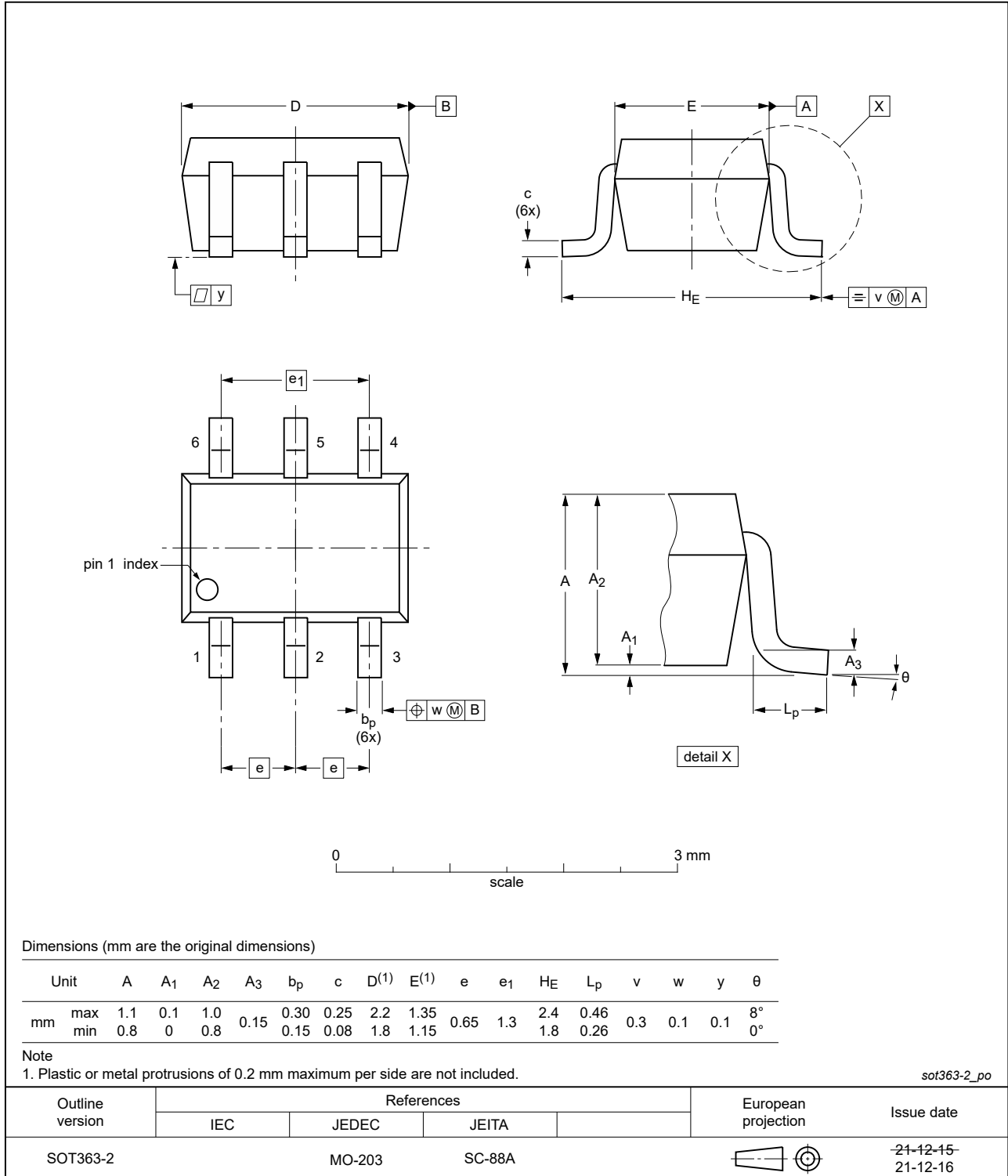


Fig. 20. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads

SOT457

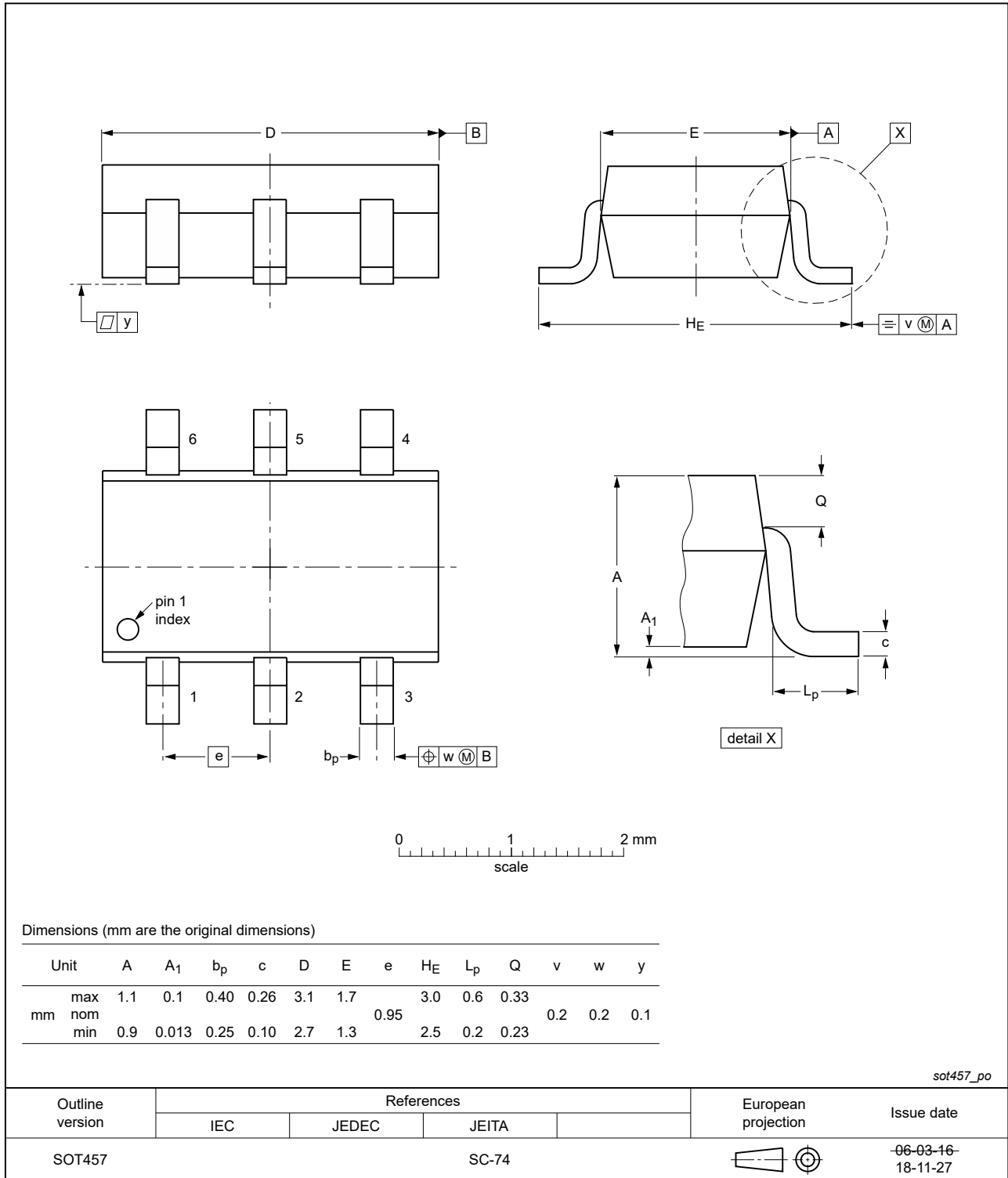


Fig. 21. Package outline SOT457 (SC-74; TSOP6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Fig. 22. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115

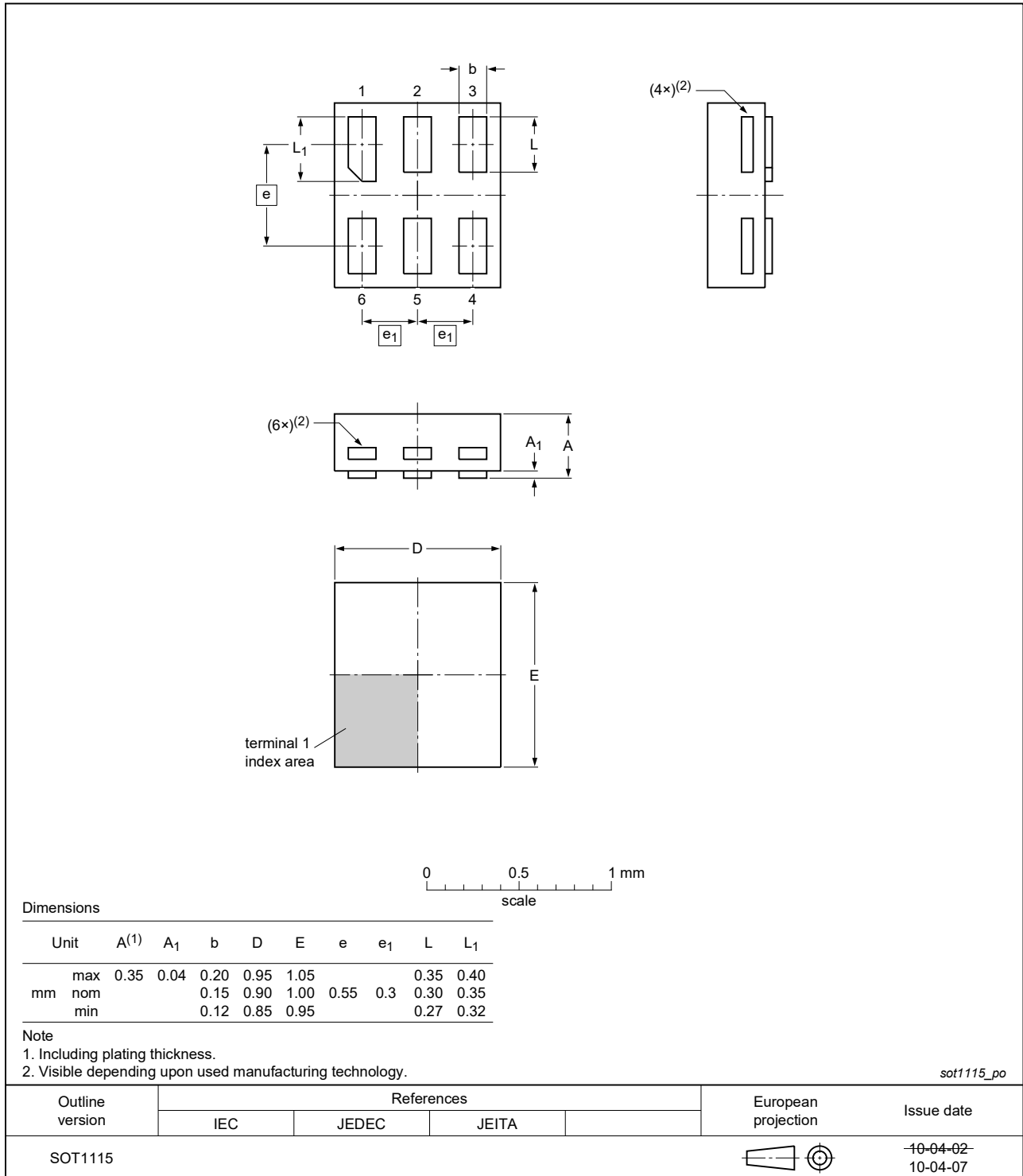


Fig. 23. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Fig. 24. Package outline SOT1202 (XSON6)

X2SON6: plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 x 0.8 x 0.32 mm

SOT1255-2

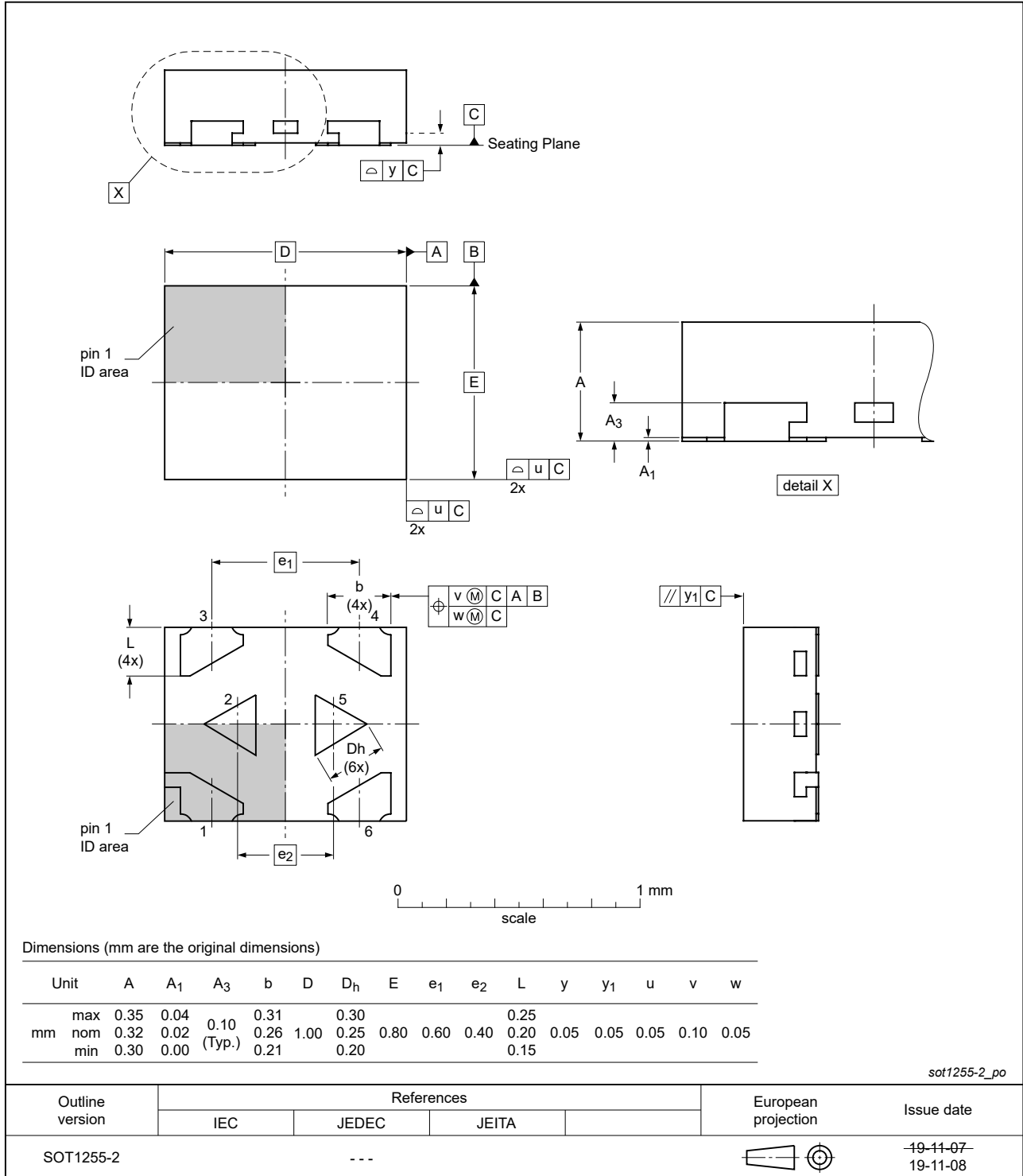


Fig. 25. Package outline SOT1255-2 (X2SON6)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G3157 v.11	20230823	Product data sheet	-	74LVC1G3157 v.10
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC1G3157 v.10	20230411	Product data sheet	-	74LVC1G3157 v.9
Modifications:	<ul style="list-style-type: none"> Package SOT1255 (X2SON6) changed to SOT1255-2 (X2SON6). Updated descriptive title in line with 74LVC2G3157. 			
74LVC1G3157 v.9	20230123	Product data sheet	-	74LVC1G3157 v.8
Modifications:	<ul style="list-style-type: none"> Type number 74LVC1G3157GF (SOT891/XSON6) removed. 			
74LVC1G3157 v.8	20220204	Product data sheet	-	74LVC1G3157 v.7
Modifications:	<ul style="list-style-type: none"> Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). Section 1 updated. Table 5: Derating values for P_{tot} total power dissipation updated. Package outline drawing SOT457 updated. 			
74LVC1G3157 v.7	20170214	Product data sheet	-	74LVC1G3157 v.6
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC1G3157 v.6	20160512	Product data sheet	-	74LVC1G3157 v.5
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G3157GX (SOT1255 package) Table 9: Minimum and maximum values enable and disable times revised. Table 12 and Fig. 17: Condition and test circuit for $f_{(-3dB)}$ revised. Fig. 19: Test circuit for charge injection revised. 			
74LVC1G3157 v.5	20121206	Product data sheet	-	74LVC1G3157 v.4
Modifications:	<ul style="list-style-type: none"> Package outline drawing of SOT886 (Fig. 22) modified. 			
74LVC1G3157 v.4	20111206	Product data sheet	-	74LVC1G3157 v.3
74LVC1G3157 v.3	20100916	Product data sheet	-	74LVC1G3157 v.2
74LVC1G3157 v.2	20070918	Product data sheet	-	74LVC1G3157 v.1
74LVC1G3157 v.1	20050207	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 23 August 2023